UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00996 (Patent 11,016,918 B2)
IPR2022-00999 (Patent 11,232,054 B2)[1]

Record of Oral Hearing
Held: September 11, 2023

Before: PATRICK M. BOUCHER, JON M. JURGOVAN, and DANIEL J. GALLIGAN, Administrative Patent Judges.

[1] We exercise our discretion to issue one Order to be filed in each of the above-identified cases. The parties, are not authorized to use this style heading in any subsequent papers.

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The above-entitled matter came on for hearing Monday, September 11, 2023, commencing at 1:03 p.m. EDT, via Video-conference.

P R O C E E D I N G S

1:03 p.m.

JUDGE JURGOVAN: This is the trial hearing for the following cases: IPR2022-00996 concerning U.S. Patent No. 11,016,918 B2 and IPR2022-00999 concerning U.S. Patent No. 11,232,054 B2.

The date is September 11, 2023. The time is 1:00 p.m. Eastern. On the panel today are APJ's Patrick Boucher, Daniel Galligan, and myself, Jon Jurgovan. Who will be speaking on behalf of the Petitioner in this case?

MR. CHANDLER: Morning, Your Honor. Ted Chandler from Baker Botts on behalf of the Petitioner, Samsung Electronics Co. Limited.

Also on the line is counsel from Micron. They're in an understudy position and won't be arguing.

But I believe they would like to introduce themselves this morning.

MR. YAQUIAN: Hi, Your Honors. This is Juan Yaquian here for Micron.

JUDGE JURGOVAN: Thank you. Who will be speaking on behalf of the Patent Owner today?

MS. ZHONG: My name is Anita Zhong from Irell & Manella. Also on the line, my colleagues, Mr. Jason Sheasby and Mr. Jonathan Lindsay. Mr. Sheasby will be doing the presentation today.

JUDGE JURGOVAN: Thank you. As stated in the hearing order, each party will have up to ninety minutes to present their arguments for both cases.

Since Petitioner bears the burden of proving its case by a preponderance of the evidence, Petitioner will begin followed by the Patent Owner.

Each party may reserve time for rebuttal limited to the opposing party's presentation.

As you address the demonstratives, papers, and exhibits in the record, please identify them clearly by page number and a paper or exhibit number so that the record will be clear what you're pointing out in your presentations.

Please identify yourselves as you begin speaking so that the court reporter will know who you are.

After the hearing, please remain on the line in case the court reporter has any questions to ask you of terms that may have been used in the hearing or other matters that may not have been understood.

As this hearing is public, third parties may be listening on the line.

None of the information in this hearing has been designated as confidential.

If for some reason you need to discuss confidential information, please let the judges know in advance so we can address the matter.

If at any time you experience technical difficulties that impair your ability to represent your client, please alert us and contact the number given you to resolve the issue.

Petitioner has filed motions to exclude in each case. The parties may devote some of their allotted time to address the motions to exclude.

However, it is unlikely we will rule on the motions to exclude today. Do the parties have any questions before we begin?

MR. SHEASBY: Yes, Your Honors. Jason Sheasby for the Patent Owner.

I did want to discuss the specific page of an exhibit that's in the record.

Do I have Your Honor's permission to use the share function to discuss that page?

(Simultaneous speaking.)

JUDGE JURGOVAN: Yes, you do.

MR. SHEASBY: Thank you.

JUDGE JURGOVAN: Share is fine. So we'll begin with the Petitioner's presentation. How much time would you like to reserve for rebuttal?

MR. CHANDLER: Thirty minutes, please.

JUDGE JURGOVAN: Thirty minutes. Okay. You may proceed when you are ready.

MR. CHANDLER: All right. I'm sharing on the screen our demonstratives marked as Exhibit 1079.

Are you able to see the demonstratives and are you able to hear me all right?

JUDGE JURGOVAN: Yes, we are.

MR. CHANDLER: Thank you. So starting on slide 5, this provides an overview of the '918 patent.

As highlighted in yellow in the upper left, the '918 patent claims priority back to an application filed on June 2nd, 2008.

Our contention is that the claims of the '918 and '054 patents are not entitled to the earlier provisional filing date of June 1st, 2007.

Patent Owner has not responded to this issue, and so we believe that June 2nd, 2008 is the relevant date for these IPRs.

On the right side of the slide is claim 1 of the ’918 patent. As highlighted in red, the claimed invention of the ’918 patent requires four converters on the memory module providing four regulated voltages.

Slide 6 provides an overview of the ’054 patent which is a continuation of the ‘918 patent as shown by the yellow highlighting. And it requires three buck converters and three regulated voltages.

Slide 7 provides an overview of the disclosed embodiment of the ’918 and ’054 patents.

Figure 12 on the left shows a memory module where the yellow is volatile memory such as DDR2 memory.

The green is non-volatile memory such as NAND flash memory. The red is controller 1062, and the blue is the power supply 1080.

Slide 8 shows Figure 16 of the ’918 and ’054 patents which provides an example of four converters on a memory module.

1122 in teal is a converter buck converter outputting 1.8 volts. 1124 in green and yellow is a dual buck converter with outputs of 2.5 volts and 1.2 volts.

And 1126 in red is a buck-boost converter outputting 3.3 volts.

Slide 10 shows the instituted grounds which are similar in those IPRs.

For grounds 1 through 3, the primary reference is Harris with grounds 2 and 3 covering all of the claims.

And for grounds 4 and 5, the primary reference is Spiers. And these grounds also cover all of the claims.

Slide 11 provides an overview of Harris which is the primary reference for grounds 1 through 3.

As shown by the red box in the middle, Harris teaches putting at least one onboard voltage regulator module on the memory module just like the ’918 and ’054 patents.

As shown on the right, paragraph 9 of Harris teaches that the onboard voltage regulator module can provide voltages from 0.5 volts up to 3.5 volts or more.

And as shown on the left, paragraph 12 of Harris specifically identifies an FBD module which stands for fully buffered DIMM module as a type of memory module that could benefit from his invention.

Slide 12 provides an overview of the FBDIMM standards which are relevant given that Harris specifically identifies FBDIMM as a type of memory module that could benefit from his invention.

As shown on the right of this slide, the FBDIMM standards identify a number of voltages required by an FBDIMM, including 1.5 volts, 1.8 volts, 3.3 volts, and 0.9 volts for VTT which is half of the primary voltage.

Slide 13 provides an overview of the Amidi reference which discloses providing battery backup for a memory module in the event that a power fault is detected.

Slide 14 provides an overview of the Hajeck reference which teaches a voltage detection circuit for detecting both undervoltage conditions as well as overvoltage conditions when the voltage exceeds a certain level.

Slide 15 provides an overview of the Spiers reference which is very similar to the ’918 and ’054 patents.

Figure 5 in the middle shows a memory module where the yellow is volatile memory, the green is non-volatile memory.

The blue are capacitors that provide backup power, and the red is an FPGA controller on the memory module.

As shown on the right side in the event that the memory module detects a power failure, the memory module can switch power to the capacitors shown in blue, also referred to as CAPS, C-A-P-S, and can transfer data from the volatile memory in yellow to the non-volatile memory in green to avoid losing any data.

Slide 18 summarizes the ground 1 combination of Harris and the FBDIMM standards.

This combination is essentially the same for both IPRs. But as shown in the bottom right, for each IPR, we provided three different ways that the voltages disclosed in ground 1 satisfy the claim 1st, 2nd, and 3rd, and 4th regulated voltages. And we refer to these as voltage mappings A to C in each IPR.

Slide 19 shows a quote from the Federal Circuit decision in *General Hospital v. Sienna*, which makes the point that, quote, when a prior art patent discloses a range of values, showing claim value falls within that range meets the party's burden of establishing the narrower claim would've been obvious when there is no reason to think the result would be unpredictable, end quote.

This precedent is important because ground 1 not only teaches the specific voltage mappings A to C shown on the bottom right.

But ground 1 also teaches more generally that any voltages within the range 0.5 volts to 3.5 volts can be generated on the module using at least one onboard voltage regulator module.

Slide 20 summarizes ground 2 which adds the teachings of Amidi shown in blue to the module of ground 1.

Amidi teaches battery backup and logic for detecting power faults.

And Amidi, like Harris, also teaches using buck converters on the memory module.

We contend that ground 2 renders obvious all claims of the ’918 and ’054 patents.

Slide 21 summarizes ground 3 which adds the teachings of the Hajeck reference shown at the bottom. As shown in red, Hajeck teaches a voltage detection circuit that monitors for overvoltage conditions such as power surges and spikes as well as undervoltage conditions including power outages.

Slides 22 through 31 address Patent Owner’s primary argument against grounds 1 to 3 which is that according to the Patent Owner, it would be non-obvious to supply power to the edge connections at the bottom of the memory module.

Slide 23 shows that the Institution Decision correctly rejected this argument.

Slide 24 shows that Harris teaches replacing the standard power supply interface pins which are along the bottom edge of the memory module with fewer 12-volt pins.

Paragraph 2 of Harris in the upper left teaches that standard memory modules in the prior art needed a, quote, relatively large number of pins, end quote, to supply all the different voltages required by the memory module.

Now it’s undisputed that it was standard in the prior art for power to be supplied to the pins along the bottom edge of the memory module.

Paragraphs 10 and 12 of Harris propose replacing those large number of pins along the bottom edge with as few as six 12-volt pins.

Paragraph 14 of Harris emphasizes that his invention works with any combination of known and heretofore unknown voltage supplies.

Again, it's undisputed that it was known that standard memory modules like an FBDIMM receive power from the pins along the bottom edge of the memory module.

And that's our contention is that it would've been completely obvious from the teachings of ground 1 to continue to use power pins along the bottom edge of the memory module.

Slide 25 shows at the top that Netlist expert admits that it was, quote, standard for a memory module to receive power from the edge connections along the bottom edge of the memory module.

For example, as shown in the middle of this slide, it's undisputed that FBDIMMs receive power from the edge connections along the bottom of the memory module.

And as shown at the bottom of this slide, Harris specifically identifies FBDIMM as a type of memory module that could benefit from his invention.

I have a few additional slides in support of our argument that will be obvious to supply power along the bottom.

But in the interest of time, I was planning to move on to the next issue unless the Board has any questions for me on this issue.

Moving on to slide 32, slides 32 through 37 address the Patent Owner's second argument against grounds 1 through 3 which is that according to the Patent Owner, it would be non-obvious to use data, address, and control signals between the memory module and the host system.

Slide 33 says that the Institution Decision correctly found that ground 1 renders those signals obvious as shown on the right side of slide 33.

For example, Harris on the left teaches that the buffer in red on the memory module receives data, address, and control signals via memory control or interface 114 highlighted in yellow.

Slide 34 shows on the left the layout of an FBDIMM memory module.

And again, Harris is an example of an FBDIMM memory module.

In the middle of the FBDIMM memory module is a box labeled AMB which stands for advanced memory buffer.

As shown at the bottom of the drawing, the memory controller in the host computer sends address command and clock signals to the AMB as well as DQ data signals and DQS strobe signals.

And as explained by Netlist's expert on the right side of this slide, these signals sent from the host to the AMB are sent as packetized serial signals.

But they are still signals which is all that the claims of the '918 and '054 patents require.

Slide 35 provides more detail about how the AMB buffer on an FBDIMM memory module works.

As shown in the upper left, the JEDEC standard for the AMB makes clear that it is the host computer that is in charge of, quote, all memory control for the DRAM including memory request initiation, end quote.

In other words, it's the host that determines what data signals to send, what address signals to send and what control signals to send.

As underlined in red on the left, the JEDEC standard makes clear that the host sends those, quote, signals to the AMB, including the signals labeled PS0 to PS9 which are high speed serial signals.

As confirmed by Netlist's expert on the previous slide, the signals from the host include data, address, and control signals sent as packetized serial signals.

The AMB then decodes those signals and sends corresponding data, address, control signals to the DRAM memory devices as shown on the right side of this slide.

Slide 36 responds to one of Netlist's arguments. Netlist's argument as shown on the right is that the claims require dedicated pins for data, address, and control signals.

According to Netlist, encoding signals so they can be sent in packets as is done with the FBDIMM memory module somehow does not satisfy the claim language.

But as shown on the left, the claim language just requires signals, not a dedicated pin for each signal.

Slide 37 shows that Netlist's argument would exclude FBDIMM from the scope of the claims which is contrary to disclosure in the '918 and '054 patents on the left which explicitly identifies FBDIMM as the preferred embodiment.

And as explained by the Federal Circuit on the right the claim construction that excludes the preferred embodiment is rarely if ever correct and would require highly persuasive evidentiary support.

Slides 38 through 62 address Patent Owner's third argument against grounds 1 through 3 which is that according to patent owner, it would be non-obvious to use three or four buck converters on the memory module.

Slide 39 shows the Institution Decision correctly rejected Netlist's argument and found that it would be obvious in light of ground 1 to use four buck converters on the memory module.

Slide 40 shows that it was well known to use buck converters to provide a lower regulated voltage.

The upper left is paragraph 10 of Harris which teaches the use of a, quote, switching voltage converter on the memory module which as shown by the textbook on the right is called a buck converter when you're going from a higher voltage to a lower voltage.

The lower left figure is Figure 6 of the Amidi which explicitly uses the label buck for a converter that goes from 3.6 volts down to 1.8 volts.

Slide 41 shows in the upper left that Netlist expert admits that buck converters were known in the art.

And as explained by our expert on the bottom left, the trend in the industry was to use buck converters in part because they are highly efficient as we explained on the right in the petition.

Slide 42 quotes two Federal Circuit decisions which are relevant to many of the arguments that Netlist makes.

I will discuss Netlist's arguments in more detail in the following slides.

But first I want to make an overall point. Netlist repeatedly argues that instead of using a buck converter, you could use something else like an LDO regulator.

The problem with Netlist's arguments is that as a legal matter, they miss the mark.

The Federal Circuit has repeatedly emphasized that for purposes of obviousness, it does not matter if a buck converter is considered inferior in certain situations or if there are better alternatives to a buck converter in certain situations.

Rather as shown on the right, the question is whether a buck converter was a suitable option.

Here, the answer is yes. A buck converter was a suitable option.

Harris and Amidi both specifically taught using buck converters.

Buck converters were taught in textbooks, and they were widely used and commercially available at the time.

In short, it was obvious to use buck converters to provide lower regulated voltages on a memory module.

Slides 43 to 49 respond to Netlist's argument that Harris only teaches using one buck converter and that it would therefore be non-obvious to use four buck converters for four different voltages.

Slide 43 on the left quotes from Netlist's brief which points to a single sentence in paragraph 10 of Harris that refers to, quote, a high frequency switching voltage converter, end quote.

That is shown in the upper right of this slide, paragraph 10 of Harris, as well as claim 1 of Harris made clear that the invention is not limited to a single voltage converter and instead also works with multiple voltage converters which is why Harris repeatedly uses the phrase, quote, at least one onboard voltage regulator, end quote.

Slide 44 points out another problem with Netlist's argument. As shown on the left, Netlist argues that Harris' voltage regulator module shown in the red box is a single buck converter that outputs two different regulated voltages, VCC which is 1.5 volts in Harris and VDD which is 1.8 volts.

But as shown on the right, the problem with Netlist's argument is that what Netlist is calling one buck converter is actually two buck converters according to the '918 and '054 patents given that they're two different regulated voltage outputs.

It doesn't matter that Harris draws one box for the voltage regulator module.

What matters is the number of regulated voltage outputs. And we know from the FBDIMM standards that Harris would need to provide four different regulated voltage outputs, thus making it obvious to use four buck converters.

Slide 45 shows that a single chip such as the one shown on the left can include multiple buck converters as admitted by Netlist's expert on the right.

Again, the point is it does not matter that Harris shows only one box for the voltage regulator module because that one box can have multiple buck converters.

Slide 46 shows that it was common for a single chip to have multiple buck converters.

And such chips were commercially available. Slide 47 shows that it was also common to use multiple buck converters for multiple outputs.

In this example, the input is 12 volts as highlighted in yellow just like in Harris.

And there are three different buck converters shown in red outputting three different regulated voltages, 3.3 volts, 2.5 volts, and 0.9 volts.

Slide 48 responds to an argument by Netlist as supposedly there would not have been enough space on a memory module to fit four buck converters.

But as shown on the left, paragraph 13 of Harris teaches that one square inch on both sides of the printed circuit board would be enough space for all the voltage conversion contemplated by his invention.

And as shown on the right, our expert confirmed that buck converters can be extremely small.

Furthermore, nothing in the ’918 or ’054 patents suggest that space was a concern.

And there’s nothing in the claims of the ’918 or ’054 patents that limit the amount of space available for the buck converters.

So if you need to make the memory module a little bigger to fit four buck convertors, that would still satisfy the claims of the ’918 and ’054 patents.

Slide 49 shows that another reason to space for buck converters was not a concern is because it was known that you could stack DRAM memory chips to save space on the board.

As Netlist’s expert admitted in the right, when you stack the DRAM memory chips, quote, you’ve now doubled the amount of memory stored in the same amount of physical space, end quote.

That was a known option at the time to save space on the memory module.

Slides 50 to 52 respond to Netlist's argument that it would be non-obvious to use two different buck converters or two different voltages.

Slide 50 on the left shows that this argument by Netlist is relevant to voltage mappings A and B and not voltage mapping C, though, because voltage mapping C uses four different voltage levels ranking from 0.9 to 3.3 volts.

With respect to voltage mappings A and B, the Institution Decision on the right correctly rejected Netlist's argument and found that it was obvious to use two different buck converters for the same voltage to provide, quote, independence for the power supplies with improved stability and flexibility for power management, end quote.

Slide 51 shows two excerpts from the JEDEC standard on the left side.

As shown by the blue and red highlighting, JEDEC teaches two different options for VDD, VDDL, and VDDQ.

One option as shown in blue is to use a, quote, single power converter, end quote, for those three voltages.

But another option shown in red is to use multiple converters to permit independent control and isolation of those voltages. As explained, our --

JUDGE JURGOVAN: Can I ask a question here?

MR. CHANDLER: Please.

JUDGE JURGOVAN: I believe Patent Owner's argument with respect to the red box is that these are just singular sentences.

And there's no conjunction that all of these things would be used together. But how do you respond to that argument?

MR. CHANDLER: That's incorrect, Your Honor. As you see the bottom there, it says, at least one of these two sets of conditions must be met.

And the two sets are the one sets above or which we've underlined in red. And the other set is below the or.

Also, in the second red box below that, there's a second indication in the same JEDEC standard that is recommended to isolate VDDL from VDD and VDDQ which is consistent with how we are interpreting the two sets, the two options.

And then furthermore as explained by our expert at the bottom, it would be obvious that you would want to treat those voltages independently so that you could sequence the power so that you could turn the power on and off independently.

And also, because it may be more cost effective to use multiple small regulators rather than one large regulator.

JUDGE JURGOVAN: Thank you.

MR. CHANDLER: The second option in red is consistent with sequencing the power as explained by our expert.

And that would be a motivation for having separate buck converters.

The second option requires that the VDD, for example, is turned on before or at the same time as VDDL.

And so you would need separate buck converters for that capability to sequence the order in which you power up these different voltages.

Slide 52 cites to additional evidence supporting the point that they were known advantages using multiple buck converters, even if they all output 1.8 volts.

And again, those advantages include sequencing, independent control, efficiency, and saving power.

Slides 53 through 57 respond to Netlist's argument that it would be non-obvious to use a buck converter on the module for VTT.

Slide 53 on the left shows that this argument is only relevant to voltage mapping C which includes a VTT voltage of 0.9 volts.

As shown on the right side of Slide 53, the Institution Decision correctly rejected Netlist's argument and found that it would logically follow to generate VTT on the module using the same voltage regulatory module 102 as used to generate voltages VCC and VDD.

Furthermore, the Institution Decision correctly reasoned that, quote, there are only two options.

Generate the voltage VTT on the module as Petitioner indicates or obtain the voltage VTT from the interface pins, end quote. And thus under KSR, either option would've been obvious.

Slide 54 shows that Harris teaches generating all of the needed voltages on the module which would include VTT.

Now Netlist argues that Harris does not explicitly illustrate VTT in Figure 1A in the upper left of this slide.

But Harris teaches replacing all the power supply pins on an FBDIMM memory module with fewer 12-volt pins.

And then as shown at the bottom in green, a standard FBDIMM needs power supply pins for VTT.

It would thus be obvious in light of Harris' teaching to eliminate the power supply pins for VTT and instead to use a buck converter to generate VTT on the memory module.

Slide 55 shows that buck converters were commercially available that were suitable for generating VTT.

But not only was it obvious to use a buck converter for VTT, it was common.

Slide 56 shows that it was known that buck converters were generally more efficient than an LDO regulator at converting from 12 volts down to 0.9 volts as would be required for VTT.

JUDGE JURGOVAN: Counsel, can I interrupt for a second? So are dual buck or rather are buck converters and LDOs the only options for converters to use in this context?

MR. CHANDLER: The only two that the parties have discussed and they're the two that I recall seeing in the record.

In the provisional, there is reference to a third type, something like a transformer. But all the discussions been around buck convertors and LDOs.

JUDGE JURGOVAN: And then the high-speed switching voltage converter, I think that's how Harris describes what its converter is.

MR. CHANDLER: Yes.

JUDGE JURGOVAN: How would one know with certainty that that's a buck convertor and not some other kind of converter? Are buck converters the only converters that use switched --

MR. CHANDLER: Yes.

JUDGE JURGOVAN: -- voltages that they're input?

MR. CHANDLER: Yes, that's the description. So we have this here on slide 40.

So the textbook that we show on the right says that there are three typical MOSFET switching regulator circuits.

The word, buck, just means you're going from high to low. If you're going from low to high, it would be called boost.

But when you're talking about a switching converter, the textbook example is a buck converter. They go from high to low.

And we also have additional citations for that point in the petition.

So we've got four or five citations to several different textbooks about how a buck converter is what is understood as a switching voltage converter when you're going from high to low.

And here we're going from 12 volts is what Harris teaches to a range of lower voltages, 0.5 volts, 3.3 volts. And so that would be a buck converter.

JUDGE JURGOVAN: Thank you.

MR. CHANDLER: And of course, Amidi in the bottom left also calls it a buck converter.

So getting back to slide 56, as admitted by Netlist's expert on the left, buck converters generally have higher efficiency than an LDO.

As explained by Netlist's expert on the bottom left, if you have an LDO and the input is 10 volts and the output is 1 volt, then you divide 1 by 10 and that results in an efficiency of only around 10 percent.

As explained on our expert on the right, the efficiency levels for buck converters can be much higher in the range of 80 to 90 percent.

As a result, the trend over the years has been to move all computer power supplies to buck converters.

Slide 57 shows that Netlist's suggestion of generating VTT on the motherboard would defeat the benefit of Harris' invention.

As explained by paragraph 12 of Harris on the left and paragraph 19 of Harris in the middle, the benefit of generating all the voltages on the memory module instead of relying on the motherboard is that you don't need to keep changing the power supply on the motherboard every time a new generation of memory devices comes out that uses a lower voltage.

As shown on the right, each new generation of memory devices has use of lower voltage from 2.5 volts for DDR1 and 1.8 volts for DDR2 and now 1.5 volts for DDR3.

As previously shown on slide 54, the VTT voltage is one-half of the primary voltage meaning that VTT also changes with each new generation of memory devices.

So VTT changes from 1.25 volts for DDR1 down to 0.75 volts for DDR3.

Thus, it would defeat the benefit of Harris' invention to generate VTT on the motherboard as suggested by Netlist.

And instead, the obvious thing to do based on the teaching of Harris would be to generate VTT on the memory module.

Slides 58 through 62 respond to Netlist's argument that it would be non-obvious to use a buck converter on the memory module for VDDSPD.

Slide 58 on the right shows the Institution Decision, correctly rejected Netlist's argument, and found that, quote, it would've been obvious to one of ordinary skill to use multiple converters including well known buck converters to generate the four voltages needed, end quote.

Slide 59 show that Netlist never argues that the claims require the fourth converter to be a buck converter.

As shown in yellow, the claims explicitly state that the first, second, and third converters must be buck converters.

But as shown in blue, the claim just says converter, the fourth voltage.

And Netlist never argues that this converter must be a buck converter.

We've shown that it would be obvious to use a buck converter or VDDSPD, thus satisfying the claim language for the fourth converter.

But it's important to remember that all of Netlist's arguments in favor of using an LDO for VDDSPD do not help Netlist's position because Netlist never argues that an LDO would be insufficient to satisfy the claim language for the fourth converter.

Slide 60 shows that it was known the buck convertors were generally more efficient that LDO at converting from 12 volts down to 3.3 volts as would be required for VDDSPD.

As shown on the upper right and as previously discussed, if you use an LDO to go from 12 volts down to 3.3 volts, that would result in an efficiency of about 3.3 divided by 12 or about 28 percent.

But as explained by our expert on the lower right, buck converters are generally much more efficient than an LDO even at very low currents.

Slide 61 shows that Netlist's suggestion of generating VDDSPD on the motherboard would defeat the benefit of Harris' invention which is to provide technology independence by generating all of the voltages on the memory module so you don't need to change the motherboard every time a voltage on the memory module changes.

Slide 62 shows that Netlist's suggestion of generating VDDSPD in the motherboard would also defeat the benefit of ground 2 which is to have battery backup available for all the voltages needed by the memory module in case there's a power fault.

In the interest of time, I'm going to skip ahead to slide 68. Slide 68 through 75 respond to Netlist's arguments that overvoltage protection was not obvious for grounds 2 and 3.

Slide 69 shows that the Institution Decision correctly found that overvoltage protection was obvious in light of grounds 2 and 3.

Slide 70 explains the motivation for overvoltage protection which is to avoid damage and data loss on the circuit.

And again, anyone who has a surge protector at home knows that power surges and spikes are a problem and can cause damage and data loss.

And so there was a motivation, a known motivation, to provide overvoltage protection.

Slide 71 shows that both overvoltage protection and undervoltage protection was obvious and common as shown by commercially available products on the left and the upper right and the patent application cited on the bottom right.

Slide 72 shows the references in grounds 2 and 3 that render obvious both overvoltage and undervoltage protection.

Harris on the left states that his memory module and only, quote, accommodate, end quote, an input voltage that varies by plus or minus 15 percent.

This provides a motivation to detect any voltage that exceeds 15 percent because such a voltage cannot be accommodated and instead could cause damage.

Amidi in the middle teaches power fault protection which is not limited to power outages.

And then Hajeck on the right expressly teaches a voltage detection circuit that can detect both voltages below a certain level and voltages that exceed a certain level.

And Hajeck states in the middle that, quote, a conventional voltage detection circuit may be used, end quote, confirming that this technology was common as I showed on the previous slide.

Slide 73 shows Amidi specifically discloses the trigger signal called the result signal in the event of a power disruption.

And then slide 74 shows that Hajeck also specifically discloses a trigger signal called the busy signal in the event of an overvoltage condition.

Hajeck explains in the upper left that surges and spikes can cause permanent damage.

So Hajeck teaches a voltage detection circuit 48 that sends a busy signal so that the memory module can switch to backup power such as the battery 52 shown below in Figure 1. Slide 75 shows the testimony --

JUDGE JURGOVAN: Counsel, can I interrupt for a second?

MR. CHANDLER: Yes.

JUDGE JURGOVAN: So the generating a busy signal, is that really providing protection from an overvoltage condition?

MR. CHANDLER: A couple responses. The answer is yes, trigger signal.

And it's the busy signal that tells the memory subsystem to shut down. And that's what we get at on slide 75 to protect the data.

Also, remember that Hajeck is being combined with Amidi. And Amidi also has this trigger signal as shown on slide 73.

And as shown on the right side of slide 73, Amidi teaches what you do in response to the trigger signal, how you transition the memory module to battery backup power.

And you put the memory in self-refresh mode to conserve power.

But to answer your question, Hajeck also teaches that, that the busy signal is what is going to pause the memory device -- memory module to switch to the optional battery backup. And that's --

JUDGE JURGOVAN: Thank you.

MR. CHANDLER: -- further explained on 75.

JUDGE JURGOVAN: Thank you.

MR. CHANDLER: So slide 75 shows the testimony of our expert explaining how Hajeck would work in the event of an overvoltage condition.

As explained on the right when there's an overvoltage condition, Hajeck discloses an embodiment where the battery takes over to provide enough time to complete any outstanding memory operations before shutting down.

Slide 76 through 79 address the dependent claims of the '918 patent that require a write operation.

Slide 77 summarizes the petition which explains that grounds 2 and 3 use the battery powered logic in Amidi shown in blue both in the title and on the left side of Figure 1A.

The battery powered logic is used to switch to S3 sleep mode in the event of a power disruption.

And the power disruption as shown in the upper left, this battery powered logic is on the memory module in grounds 2 and 3.

So the power disruption affecting the host computer will not affect the logic's ability to switch to S3 sleep mode.

Slide 78 shows on the left that when entering S3 sleep mode, various information is written to non-volatile memory before the DRAMs are put into self-refresh mode as explained on the right.

And the reason for doing that is later on when the power is restored, the information written to non-volatile memory can be used to get the DRAMs out of the self-refresh mode and back to normal operation.

And slide 79 is just a reminder that you need overvoltage protection in grounds 2 and 3 to avoid damage and data loss.

In the interest of time, I'm going to skip again to grounds 4 and 5.

So slide 92 provides an overview of the ground 4 combination of Spiers and Amidi which we contend renders obvious all claims of the '918 and '054 patents.

As shown in the top, Spiers is very similar to '918 and '054 patents.

Spiers teaches a memory module outlined in red that can transfer data from the volatile memory shown in yellow to the non-volatile memory shown in green using backup power from capacitors shown in blue in the event of a power disruption.

And then Amidi as summarized in the bottom left is similar to Spiers because it's also directed at providing backup power for memory module.

As shown at the bottom right, there are two voltage mappings A and B for the '054 patent and three voltage mappings A through C for the '918 patent.

Voltage mapping A uses the voltages for DDR3 memory devices which were known by 2007.

And voltage mappings B and C use the voltages for DDR2 memory devices which are the preferred embodiment in Amidi.

Slide 93 is a reminder about the Federal Circuit case law that I discussed earlier which is also relevant here.

Slide 94 provides an overview of the ground 5 combination which adds the teachings of Hajeck about overvoltage and undervoltage protection.

Slides 95 to 106 respond to Netlist’s argument that Spiers did not disclose a, quote, memory module.

It’s important to remember that ground 4 combines Spiers with Amidi.

Netlist does not dispute that Amidi discloses a memory module. But as I will explain, Spiers also discloses a memory module.

Slide 96 shows that the Institution Decision directly found that Spiers discloses a memory module shown in red on the left as 144.

And that memory module has both volatile memory shown in yellow and non-volatile memory shown in green.

Slide 97 responds to Netlist’s claim construction argument. According to Netlist, the term, memory module, should be construed and limited to a, quote, main memory module.

Neither the Board nor the District Court limited a memory module to a main memory model.

Instead, they both nearly held that the preamble was limiting without further limiting the claim term, memory module.

Slide 98 shows the page of the District Court that Netlist points to.

But nowhere does this page say anything requiring that the memory module be limited to a main memory module.

In particular, Netlist points to this sentence towards the bottom that a memory module includes the structure necessary to connect to a memory controller.

But nothing in that sentence refers to main memory a main memory controller.

Slide 99 shows that our expert agreed with the ’918 and ’054 patents’ use of the term, memory module, broadly and merely state a memory module is a board that connects to a host computer. There’s no mention here of main memory.

Slide 101 shows that the PCI card in Spiers satisfies the District Court’s comments about a memory module because as shown in the upper left, Spiers discloses a storage controller 132 which is a type of memory controller.

And that memory controller connects via bus 128 to the PCI card 144.

And as explained on the right in the middle and at the bottom, the PCI bus was specifically designed to be compatible with memory systems.

Slide 102 shows in the upper right that our expert agreed that 132 in Spiers is a memory controller.

Slide 103 shows on the right that our expert agrees that the PCI card in Spiers is a memory module.

Slide 104 responds to an argument by Netlist that the memory controller in Spiers supposedly would be processor 198 at the bottom in red rather than storage controller 132.

That's incorrect. The memory controller is on the host computer as shown by the green box.

And that is true regardless of whether the memory module also has its own controller as shown by the red box.

For example, as shown in the upper left, a common example of a memory module is an FBDIMM like Harris.

Netlist does not dispute that the FBDIMM in Harris is a memory module.

And as shown in the upper right, the '918 and '054 patents specifically identify an FBDIMM as a preferred embodiment of the invention.

This is significant because an FBDIMM has a controller on the memory module just like Spiers has processor 198 on the memory module.

But that does not change the fact that the host still has a memory controller highlighted in green.

And it's the memory controller on the host computer that calls the shots with respect to reading and writing data to and from the memory module.

Slide 105 again makes the point that even though processor 198 in Spiers is on the memory module, the host computer still has a memory controller such as 132.

And it's the memory controller that sends data, address, and control signals across the 64-bit PCI bus to the SDRAM memory devices on the memory module.

Now some of those signals from storage controller 132 may get translated by processor 198 similar to what happens in an FBDIMM.

But it's still the memory controller on the host as calling the shots.

Slide 106 shows that PCI cards were used as memory modules. Again, as shown on the bottom left, the PCI bus was specifically designed to work with memory modules, including FBDIMM memory modules which as discussed before are a preferred embodiment in the '918 and '054 patents.

Slides 107 to 115 explain why it was it obvious to use three or four regulated voltages for grounds 4 and 5, especially in light of the DDR2 and DDR3 memory devices that were standard by 2007.

Slide 108 shows the Institution Decision correctly found that grounds 4 and 5 render obvious or regulated voltages and voltages required for DDR2 and DDR3.

Slide 109 shows on the right some of the voltages required by the DDR3 standard, including 1.5 volts for VDDQ and VDD and half of that which is 0.75 volts for VTT.

Slide 110 shows on the right some of the voltages required by the DDR2 standard such as 1.8 volts per VDDQ, VDDL, and VVD and half of that which is 0.9 volts per VTT.

Slide 111 shows some relevant quotes from the Federal Circuit. On the left is a quote from *Intel v. Qualcomm* that there is an implicit motivation to combine to make a device more desirable, for example, because it is faster or more efficient.

That quote is important because it explains why there would be a motivation to use DDR2 or DDR3 memory devices which are both faster and more efficient than DDR1 and other older memory devices.

And then on the right is the quote from *Intel v. PACT XPP* that it's not necessary to show that a combination is the best option, only that it'd be a suitable option.

And that's important because DDR2 and DDR3 were fairly suitable options for memory devices at the time of the '918 and '054 patents. In fact, they were the standard for memory devices.

Slide 112 shows that using DDR2 or DDR3 memory devices with Spiers would improve both efficiency and speed.

As shown in the upper left, DDR2 and DDR3 use lower voltages than older generations of memory devices and they used less power and were more efficient.

As shown on the bottom left, DDR style memory devices were used in about 80 percent of all electronic systems confirming that they were clearly a suitable option.

And then as shown on the right, our expert provided many reasons that a person would've been motivated to use DDR2 or DDR3 memory devices rather than older memory devices, including reasons of faster speed, lower cost per bit, lower power, and greater availability since they were the mainstream memories by the time of the '918 and '054 patents in 2008.

Slide 113 shows that Netlist expert agreed that there would be a motivation to use memory devices with a lower voltage like DDR2 and DDR3 because that would lower the power consumption.

So even though Spiers Figure 5 discloses a regulator outputting 3.3 volts, there would still be a motivation to use DDR2 or DDR3 at 1.8 volts or 1.5 volts given the power savings.

Slide 114 responds to the Netlist argument that the PCI bus supposedly was too slow to take advantage of the speed of DDR2 and DDR3 memory devices.

First as explained on the previous two slides, there are other motivations besides just speed to use DDR2 and DDR3, including lower cost per bit, lower power, and greater availability since they were the mainstream memory devices by 2008.

And second, as shown on this slide on the right, by the time of the ’918 and ’054 patents in 2008, there had been improvements to the PCI bus that permitted it to operate at much higher speeds such that the PCI bus would not necessarily be a bottleneck when using DDR2 or DDR3 memory devices.

Slide 115 responds to the Netlist argument that Spiers is only for writing the memory and not for reading the memory.

That’s incorrect as shown on this slide. On the left is the PCI standard which shows that PCI cards like Spiers can both read and write to memory.

And on the right side is Figure 9 of Spiers which shows that the memory controller in Spiers will both read and write to the memory module.

Slides 116 through 127 explain why it was obvious to use three or four buck converters for grounds 4 and 5.

Slide 117 shows the Institution Decision correctly found at grounds 4 and 5 render obvious using three or four buck converters.

Slide 118, this is similar to what we discussed before that buck converters were well known at providing lower regulated voltages. And Slide 119 --

JUDGE JURGOVAN: Four minutes, Counsel.

MR. CHANDLER: Pardon me?

JUDGE JURGOVAN: Four minutes --

(Simultaneous speaking.)

JUDGE JURGOVAN: -- before you're eating into your rebuttal time.

MR. CHANDLER: All right.

JUDGE JURGOVAN: You can proceed, but you'll be eating into your rebuttal time after four minutes.

MR. CHANDLER: I'll stop here just at slide 119, a reminder that buck converters are highly efficient. Thank you.

JUDGE JURGOVAN: Thank you.

MR. SHEASBY: Your Honors, give me one moment. I'm just going to share my screen. Can Your Honors see the slide presentation on the screen?

JUDGE JURGOVAN: Yes, we can.

MR. SHEASBY: Your Honors, I would like an hour of time and then I'll reserve 30 minutes.

JUDGE JURGOVAN: Thank you.

MR. SHEASBY: May it please this honorable Board. I want to begin out of order with one of the limitations that in substantially similar form are in each of the independent claims, both the '918 and '054 patents.

And it talks about four regulated voltages, each providing a physically separate voltage.

And I know that my brother said, quote, what matters is the output.

What matters is not the output. The claim requires four physically separate regulators producing four physically separate voltages.

These are the mappings that counsel uses. And counsel's combination is Harris plus the FBDIMM specification.

Depending on how you account between 7 and 8 voltages that are used on an FBDIMM module, the assignment that counsel has presented here of arbitrarily selecting first, second, third, and fourth and shuffling in a small subset of the voltages is hindsight bias that uses the claims as a roadmap, not going from what the prior art would actually teach.

How do I know that? Well, I've done a number of PTAB arguments.

And though I envy the power and authority of ALJs, I don't envy the trouble of putting oneself back in the mindset at the time of the invention.

We're in a very, very unique situation here. It's unlike any situation I've seen before in an argument which is that the Petitioner's combination is Harris plus FBDIMM specification.

Harris combines those two. If you look on slide 33 and you focus on paragraph 9, below the yellow highlighting, quote, in the illustrated embodiment of Figure 1, for instance, the DIMM configuration, the memory module A is exemplified as a fully buffered DIMM.

Harris modifies a fully buffered DIMM according to the JEDEC specification, the exact combination that is at issue in this case.

And what does Harris do? Does Harris feed 7 voltages onto the module?

Does Harris feed 8? Does Harris feed 4? Does Harris feed 3? No.

Harris feeds a VCC and VDD and that's it. That's all Harris feeds.

The answer as to whether it was obvious to put more than one regulator on a module from FBDIMM has been answered definitively by Harris itself.

I want to show Your Honor another passage from Harris. This is paragraph 12, once again making clear that the embodiment -- so this is Harris.

This is paragraph 12 of Harris making clear that the embodiment is to modify a standard FBDIMM module.

And how do you do that? You do that for VDD to the DRAM and VCC to the buffer logic.

This language is incredibly important. Harris knew what the JEDEC specification described.

Harris knew the JEDEC specification described VTT and Vref and VCC, VDDSPD -- sorry, VCCSPD and all of these other voltages that are applied to the various components on the module.

And Harris was explicit. What I'm going to do is I'm going send VDD to the DRAM and I'm going to send VCC to the buffer logic which is the advanced memory buffer on FBDIMM.

That is what Harris taught. This argument about doing VTT on module, about doing VCCSPD on module, that is hindsight bias that is contradicted expressly by what Harris says.

There is another argument that was made that Harris is labile in a number of modules -- voltage regulator modules that can be put on the memory module.

Harris is labile but not in the way that was represented by Petitioner.

This is slide 74, looking at paragraph 14 of Harris. What Harris speaks about is not that there will be multiple voltage regulator modules supplying voltages in addition to VCC and VDD.

What Harris speaks about is that there will be backup. In other words, Harris may feed more than one 12-volt voltage for more than one source onto the module.

And in that situation, there will be a plurality of onboard VRMs for redundancy.

Harris doesn't speak about creating a plurality of onboard memory modules to supply more than VDD and more than VCC to an FBDIMM.

They're redundancy to have other ways of supplying VDD and VCC.

JUDGE JURGOVAN: Counsel, I understand your argument that you're saying that basically Harris is generating two voltages.

But wouldn't a person of ordinary skill in the art understand that, well, if I need three voltages, I'll use three converters.

If I need four, I'll use four. And that buck converters would be one option to use there.

In other words, this is sort of the *In re Harza* case where duplicating an element doesn't necessarily make it patentable. How do you respond to that argument?

MR. SHEASBY: Sure, Your Honor. So there's a couple issues to that, and I'll do it in reverse order.

So my brother spoke about the fact that all there is, is buck converters and LDOs.

That is, of course, not an accurate statement. If you go -- we talked about this on slide 68 and 69 of our presentation as well as in the argument.

Buck converters, LDO, and also Harris speaks about the fact that there are PWMs, the large number of ways of decreasing voltages besides just buck and LDO.

JUDGE JURGOVAN: Are PWMs the switching voltage regulator?

MR. SHEASBY: They are described as a switching voltage regulator by Harris, Your Honor.

They're described in Harris as they're switching voltage regulators.

And he points to both LDOs and pulse-width modulated controllers as two examples, and that's in paragraph 10.

So that's just the scientific issue. This idea that it's buck or LDO, that's not accurate just from a scientific standpoint.

The second thing is why is just adding more not obvious. And I'll speak to that.

The best answer I can give you is not my words, Your Honor. It's this.

This is slide 35. On the left-hand side is the DIMM connector for an FBDIMM -- the pin out for an FBDIMM.

The pin out for an FBDIMM says that there's a single voltage, VCC, coming in that will supply all species of VCC.

There's a single VDD coming in that will supply all species of VDD.

This is a specification. It cannot be departed from. And what that specification shows is that the artisan at the time believed and was taught and was instructed that there should not be multiple separate regulators for each of the voltages that are provided in the FBDIMM. That is an undesirable feature.

This is slide 37 of my demonstratives. It's looking at Exhibit 1026 at 9.

And you'll see that it references a single power converter. This is a colloquy that Your Honor had with counsel.

I'm on slide 38 in which he described an option 1 or an option 2.

And option 2 didn't require there to be a single power converter. Option 2 is a gross misreading of what this specification describes.

The language of the specification makes clear that a single power converter is always required for VDD as well as for VCC because there's only one pipe going in for both VCC and VDD.

And you see the reference to and and and with the comma. Those are obligatory.

Those must exist. At least one of two sets of conditions must be met.

The presence of a single power converter is not a condition. The two conditions are either Vref tracks VDDQ2 or 3 points below that because after the and, there's a period and then an or and then an and.

So the answer is why isn't this obvious of doing more, because it went exactly against the teaching of the JEDEC specification that they combined with.

A POSA reads Harris, reads the JEDEC specification, and takes from that the following.

You should not have more than VDD or VCC on module which is the exact opposite of what we teach.

Don't take my word for it. This is Andrew Wolfe on the top on slide 41.

And what that speaks about is the fact that the FBDIMMs used a single power converter at all times.

He's not aware of any instances in which they did not. In addition, Dr. Mangione-Smith is also not aware of any instance in which a single power converter was not used.

The distinction, I think, Your Honor, is the following. The idea that you would supply a diversity of voltages to not just the DRAM and not just the buffer.

But all the different components on a module was something that went against the exact dogma of what the references were teaching.

Look at what Harris does. Harris talks about local conversion for the DRAM, not for the module as a whole, not for the other components in the module.

And it talks about local conversion for the buffer AMB, not for the other modules.

I will say that if it is, in fact, the case that if one module -- putting one regulator on module was known, putting four physically distinct regulators for four physically distinct voltages just becomes obvious requires I would respectfully submit, Your Honor, to blink out of existence the objective fact of what happened.

It wasn't obvious. People didn't think it was beneficial. The JEDEC specification told you to use a single converter for both.

This idea that you can use multiple converters and that's all good in the JEDEC specification is belied by Exhibit 2046 at 36.

There is not separate pipes for each of the species of VDD. There is not separate pipes for each of the species of VCC.

It is an impossibility for there to be multiple converters for each of those that are feeding into those for each of the species.

Your Honor, have I -- I know you're not going to tell me you agree with me. But have I fairly answered your question?

JUDGE JURGOVAN: Well, can we go back to option 2 again? And explain to me again why this is not teaching the use of multiple voltages, regulator voltages.

MR. SHEASBY: Sure. So you see how it's a single converter --

JUDGE JURGOVAN: Right.

MR. SHEASBY: -- and and and. And and and are obligatory.

JUDGE JURGOVAN: Got it.

MR. SHEASBY: You need to have those. Then you have two options, Vref tracks VDDQ/2 or Vref and VDD and VTT have the following relationships.

It's the or that gives you the two options. There is no option for there to be multiple converters for VDD, VDDL, and VDDQ.

It's an impossibility. The reason why it's an impossibility because I see the pin outs on the JEDEC specification for FBDIMM.

There is no VDDQ pin out. There is no VDDQL pin out. It doesn't exist. There can only be one converter.

(Simultaneous speaking.)

JUDGE JURGOVAN: Okay. So in other words, the person of ordinary skill in the art would look at Harris and this specification and determine that you only need one converter.

MR. SHEASBY: Not that you only need, that that is what you should use.

So need gets into, well, maybe there's a benefit of that. It's not need.

It's required. It's required for there to be only one converter, and I'll explain to you why.

I'm on slide 42. Slide 42 is once again not me speaking. It's the evidence of Micron who's one of the Petitioners in this case.

It speaks about the fact that the DDR2 devices require a single power source for primary supply voltages and to ensure that all voltage levels track each other.

That's because the initial ramp up is less than 10 milliseconds. So the Petitioner is fond of pointing to the fact and saying that VDD can be before VDDL and VDDL can be before VDDQ and VDDQ can be before VTT and saying they can be independent.

And because they can be independent, that means it'd be obvious to have different converters.

That is the exact opposite of what the art felt. They can be independent, and the JEDEC specification allows them to be turned on independently.

But because they have to be turned on so rapidly, you use one converter to be able to meet the timing requirements.

This is Exhibit 2006 at page 4. And Dr. Mangione-Smith talks about this in his declaration at paragraph 88.

I should note that this is entirely unrebutted. So Petitioner is showing a lot of testimony from the deposition of their expert witness, none of which was in a declaration, none of which was in their petition.

But they will not show you any evidence contradicting Mangione-Smith's evidence that for FBDIMM which is a DDR2 design, you have to have it all together because if you don't have it all together, you won't meet the timing requirements.

So it's not a need to have, Your Honor. It's a must have. There are two arguments that Your Honors initiated why you said it would be obvious to have four voltages.

The first one was this document, Exhibit 1026. The reading of Exhibit 1026 that my brother gave is a gross misreading of this document.

And it's not just my opinion. It's grammar and it's reality. Look at the Micron exhibit.

Look at the fact that the pin outs do not allow for different sources for VDDL and VDDQ.

It's an impossibility what they're proposing. And a Petitioner would not say it's a nice to have thing.

The Petitioner would recognize that for FBDIMM, you cannot have more than one converter. It's forbidden.

JUDGE JURGOVAN: I'm still not seeing why it's forbidden in the standards.

MR. SHEASBY: Where would it go, Your Honor? So I'm on slide 36.

I know I'm not supposed to ask you questions. Where is the second converter?

So you have to have a VCC pipe. A lone VCC pipe has to come in to feed the entire module.

That's what FBDIMM requires. A lone VDD type has to come in to feed everything on the module.

JUDGE JURGOVAN: Well, I think what Petitioner is saying is you could have one converter generate VCC that's received, one generate VDD, one generate VTT, and so forth.

MR. SHEASBY: Well, to be clear, that's not what they're saying.

All their combinations, I'm on slide 31, Your Honor, are supplying sort of different separate voltages for different species of VDDL and VCC.

So in each of those situations and their combinations, they're splitting voltages separately for VCC and VDD.

Now the question I think Your Honor is asking is -- and you see all three of them -- all three of their combinations require VDDSPD.

JUDGE JURGOVAN: Right.

MR. SHEASBY: VDDSPD is part of VDD. The specification does not allow for there to be more than one VDD pipe coming in.

So you'd be completely contrary to the specification if you did what they're proposing.

JUDGE JURGOVAN: Well, I think what you're saying is that you can only have three, not four converters because VDDSPD is derived from VDD.

MR. SHEASBY: That's correct. There would be -- I'll speak to VTT and VDDSPD in a second.

I'm going to do this in pieces. But their first argument is that the specification for FBDIMM and DDR2 teaches separate converters.

It does not. It teaches a single power converter. That is all it teaches for VDDs and for VCCs separately.

And so at most, that would be two power converters that you would use for VCC and VDD.

JUDGE JURGOVAN: And so why is it advantageous to use multiple converters to generate voltages?

MR. SHEASBY: Why is it advantageous for the patents or why is it advantageous in the art?

JUDGE JURGOVAN: For the patent.

MR. SHEASBY: Yeah. So the patent speaks about it, and this is a situation in which -- if I can tell you this, Your Honor -- Harris is a design that is what I'll call a blue sky patent.

I don't mean any sort of derogatory nature about this. But it's not a patent that really actually ever implements anything or designs anything.

It just says, well, let's use a separate module for VDD and let's use a separate module -- let's do VDD and VCC in a module.

If you look at our patent, there is this detailed, detailed design. We actually designed this intense on module power management system that has all these different specific voltages on it.

And the reason why we did that and I don't have a slide handy on it.

But you can look at the timing diagram, Your Honor. We have a very, very specialized timing diagram where basically we have to pre-fetch data from NAND in order to have it available so that we don't have a block in time as we switch from DRAM to NAND.

And if you look at slide 19, you'll see this -- I'm sorry. Figure 19 in our patent, you'll see this excruciatingly detailed timing manner.

So it's because our timing does not require everything to ramp up at the same time as the FBDIMM does.

Our timing intentionally is delaying things so that NAND turns on dramatically in advance of DRAM, that NAND is being read dramatically in advance of DRAM so that the page is being pulled.

It's this unique design coupled with our unique timing that led us to this very aggressive design in which you would have multiple, four in particular modules on -- regulators on a module. Have I answered your question, Your Honor, barring that you --

JUDGE JURGOVAN: I think you've answered that you need to -- or that it's desirable to divide your timing on startup such that you can have these additional voltages.

But you haven't explained why it's advantageous to generate them each with a different converter.

MR. SHEASBY: Why does the patent generate them each with a different converter?

JUDGE JURGOVAN: Right.

MR. SHEASBY: Yeah, so the patent generates them each with a different converter because the timings are so precise at the time --the timings are so precise that it wants to be able to do it separately.

JUDGE JURGOVAN: So it's for independence of timing. It's --

MR. SHEASBY: That's correct.

JUDGE JURGOVAN: I see. I see. Thank you.

MR. SHEASBY: And that's the exact opposite of FBDIMM. FBDIMM wants these -- all of these things to happen immediately, 10 milliseconds or less.

Every single one of the VDD species must be turned on. That's what keeps them all together.

Our patent if you look at these excruciatingly detailed timing diagrams, we're not interested in things all turning on at the same time or turning on simultaneously. We're interested in having very precise control of --

(Simultaneous speaking.)

JUDGE JURGOVAN: I see. Did any of the claims reach this timing independence?

MR. SHEASBY: Yes, that's why there's four voltages requiring four separate physical -- four regulators requiring four separate physical voltages. That is it.

JUDGE JURGOVAN: There's no limitations addressing the timing, the voltages are engaged at?

MR. SHEASBY: So there are some independent claims that talk about when the voltages are engaged.

But the essence of it is it's having those four physically separate regulators, four physically separate regulators producing four physically separate voltages that gives you this ability to have a very, very precise timing.

JUDGE JURGOVAN: I see. Thank you.

JUDGE GALLIGAN: Counsel, this is Judge Galligan. I wanted to follow up on that. Can you turn to slide 44, one up from that?

MR. SHEASBY: Yes.

JUDGE GALLIGAN: I wanted to ask about this one. It says that you have to have independent voltage sources used for different voltages would require specific control circuitry to delay and more precisely control each voltage source's ramping rate, complexity, and cost. So does that Figure 19 control each of the voltage regulators?

MR. SHEASBY: No, it's -- each of the voltage regulators is -- having the separate voltage regulators is what gives you that timing ability.

JUDGE GALLIGAN: Right. So this says, though, that Dr. Mangione-Smith, his testimony appears to indicate that you need specific control circuitry to control the voltage sources. And I was wondering where that is in the patent.

MR. SHEASBY: Oh, that's in Figure 16, Your Honor.

JUDGE GALLIGAN: Right. I mean, is that -- yeah, so these three converters, where's all the description of how these are controlled?

MR. SHEASBY: So I would start at paragraph 12, Your Honor.

So paragraph 12 beginning at lines 24 on -- sorry, column 12 beginning at line 24 on of our patent discusses the fact that -- and we'll get to this in a second -- is we have something called a memory controller.

And that memory controller needs to be able to seamlessly and separately address every single piece of component on our design.

And our design has a huge number of components on it. It has the DRAM. It has the NAND. It has translation devices that go from DRAM that allow address mapping from DRAM to NAND.

And so enables the discussion beginning at column 12. And that discussion at column 12 is what enables Figure 19.

This is not a patent where someone had a glass of wine and wrote a specification in the evening.

This patent, the '918 and '054, this is a real design. This is a fully realized embodiment design that they've actually created with timing diagrams, with circuit diagrams.

It was a profound advance in the art to break with this dogma of VCC and VDD are the only thing you may need to regulate separately on module and to say we want to have this ability to precisely regulate not just VCC and VDD generically but anything we want using these voltage regulators.

JUDGE GALLIGAN: This is Judge Galligan. Let me follow up on that because if I look at column 29 around line 18, it says that the conversion element -- that's what you -- basically what you have in the red box there on slide --

(Simultaneous speaking.)

MR. SHEASBY: Yeah.

JUDGE GALLIGAN: -- on the screen there. Conversion element can comprise one or more buck converters and one or more of those converters may comprise a plurality of sub-blocks.

It seems like it's just saying get the voltages you need. And maybe this is what Mr. Chandler was referring to when he says, look, there's four lines coming out.

Somehow, you've got four regulators, right? I think I understood him to say if you've got four voltages coming out, you can call it a voltage regulator or four voltage regulators or whatever.

It's pumping out four voltages. So what is it -- I don't read anything in column 29 that says that implementing four buck converters versus one converter that has functionality of four buck converters within it is any inventive leap.

MR. SHEASBY: So I can answer that in a couple ways, Your Honor.

The first way to answer that is that I know it can be an inventive leap.

And the reason for that is because there is a substantial number of examples of using a single regulator to generate more than one voltage on a module.

You don't need to have four regulators to generate four voltages.

Don't take my word for it. This is Exhibit 1048. This is annotated on page 2.

I'm looking at slide 50. This is a single buck converter with one inductor.

And above it is a single buck inverter with one inductor. It produces three voltages.

A single buck converter can produce more than one voltage. This is slide 2003 -- sorry, Exhibit 2003 at 2, slide 2004 at 99.

This is page 51. This is a single buck converter producing four distinct voltages. A single buck converter producing two distinct voltages.

JUDGE GALLIGAN: And this is Judge Galligan. So I appreciate that reference.

So why is it that then saying, well, it's known in the art that you can have a single buck converter producing two voltages.

Let's just have two buck converters, produce those voltages. Where's the -- the testimony on paragraph -- slide 44 says that if you do it the way that the claim says, you have to have tons of extra stuff to control all this and it's really complex.

I don't see that in the patent necessarily. But what is -- so why is it -- why would it not have been obvious versus, okay, I can do two buck converters there?

MR. SHEASBY: So a couple issues. One, I respectfully disagree with Your Honor that says it's not in the patent.

Figure 16 is a detailed and precise drawing that shows not just -- it doesn't matter how many you put there.

It's a very precise drawing, shows exactly how you're using different voltages.

And that map, that leads to the circuitry. So I respectfully disagree.

JUDGE GALLIGAN: Yeah, this is Judge Galligan. I didn't mean to suggest that the patent does not disclose multiple buck converters.

I'm still wondering where the patent discloses the circuitry that Dr. Mangione-Smith says is required on slide 44.

MR. SHEASBY: So the circuitry to control it is the MCH discussing at column 12 because it's the MCH at column -- it's MCH beginning at column 12 that calls each of these things independently.

And by calling them independently, I can also give you some other examples.

Column 20, line -- it's column 27, line 59 is the start of the Figure 16.

You read part of it. It goes all the way to column 29, line 64. It goes into a detailed description of how it works.

Specific voltage outputs are column 29, lines 39 through 54. And it's also discussed at length about the FPGA having this ability to control all these things.

So there's a very complex logic circuit in FPGA on the module that does all this.

Does that -- I read that pretty quickly. Do I need to read that again, Your Honor, or was that sufficient?

JUDGE GALLIGAN: No, that's fine. This is Judge Galligan. Just then more to my question about why.

So the prior art shows let's say three voltages, two voltages, multiple voltages coming out of a buck converter.

Why then -- I understand you're saying there's a benefit to having multiple buck converters as opposed to one because you have more sophisticated control of something.

Would a person of skill in the art look at, for instance, just a box that has multiple voltages and say, you can never have multiple buck converters? I mean, is that -- I'm trying to understand the argument here.

MR. SHEASBY: Yeah, so that's a good question. So hindsight is 20/20.

In FBDIMM land, Harris plus FBDIMM, there was no perceived benefit to having multiple converters.

The specification for FBDIMM is expressed that it wants you to have only a single power converter.

Micron says you should have only a single power converter because it wants to tie them together.

So there was a sea change. The combination that they proposed is a combination that expressly teaches against having multiple converters for different species of VDD, the different species of VCC.

Micron's reference teaches against this. They want those things tightly together.

Now that's their first piece of argument. Their second piece of evidence, Your Honor, is this treatise.

This is Exhibit 1062. This is the second piece that you cite to in your Institution Decision.

They give three examples of when there may be a desire to have separate regulators, when there is a separate analog and digital supplies, when memory rails are running at 100 amperes, and when there needs to be separate devices at different times.

None of those apply. And so the answer is the idea of putting four separate regulators with all that complexity on a single module went against the expressed dogma of this combination.

It has none of the features that their treatise which is the other piece of evidence that you cite to supports.

And it's not just that there would be no reason to do it. There would be violence to doing it.

The form factor can tolerate about one square inch is what Harris says for the voltage regulator.

It is undisputed in the evidence that there's no testimony from Dr. Wolfe or anyone else that a POSA would believe you could even put four regulators on the FBDIMM design.

And I want to stop and say two things at this point. Our specification talks about FBDIMM.

This is at column 19, column 13, lines 7 through 14 of the '918 patent.

We're not talking about FBDIMM specification. Counsel for the Petitioner sped past something.

We were talking about the FBDIMM form factor which is the size of the module.

There is no argument or attempt by us to suggest that you should have the features of FBDIMM on our module design.

This argument that we're bound by FBDIMM, that's the scope of our claims, that's not what the specification says.

It says FBDIMM form factor. Why am I bringing that up? Because the FBDIMM form factor is something that has very specific -- because in addition to the FBDIMM form factor which is the shape of a card, for the FBDIMM specification as a whole, there are additional limits beyond the shape of the card.

There's limits on the width. So this is Exhibit 1028. There's limits on the width and thickness.

There's limits on the operating temperature that you may have. This is on 1028, page 2.

There's limits on the thickness. This is 1028, page 27. There's limits on the thermal resistance of each of the individual devices.

In fact, Harris invokes these at paragraph 13 of his argument where he talks about the fact that component height that he's creating has to be compatible with applicable JEDEC standards.

And so this idea that, oh, you just throw on as many as you want.

Harris doesn't care. Harris is open ended. First off, that contradicts Harris which says that the component heights have to be compatible with the JEDEC specification.

And I think if you just -- Dr. Mangione-Smith, Exhibit 2031 at paragraph 82 speaks at length unrebutted.

Trials happen for a reason. And his analysis is unrebutted that the intensity and the complexity of putting four regulators on an already space constrained FBDIMM would be something that a POSA would not do.

Separate from that, there are particular reasons. So I've spoken about the fact of what was the state of the art in this FBDIMM combination, one converter for VDD, one converter for VCC.

JUDGE JURGOVAN: Can I ask a question right here for a second?

Why did the prior art use only a single converter as opposed to multiple?

MR. SHEASBY: You're looking at it, Your Honor. Slide 47, that's one reason.

JUDGE JURGOVAN: It's a space issue?

MR. SHEASBY: It's space. But spaces, height, thickness, complexity, thermal envelope, that's one example that Dr. Mangione speaks of.

The second that Dr. Mangione speaks of is that the prior art needs to have everything tied closely together.

This is paragraph 88 of Exhibit 231 that you want one converter because they need to turn on so rapidly together.

This is the case for VCC and VDDL. They must turn on rapidly together.

Micron speaks about this fact, Your Honor, at Exhibit 2006, once again because they ramp up so rapidly.

You have to have them on one converter so that they can ramp up together at the same time.

JUDGE JURGOVAN: Thank you.

MR. SHEASBY: Yes. Okay. So we talked about how this idea of using multiple converters through the VDD, multiple converters for the VCC is exactly anathema of what the state of the art was.

But I now want to engage -- we talked about there are two pieces of evidence for this which is the JEDEC specification and the treatise which both don't support them.

I now want to engage I think more precisely the issue of VTT because there's an argument --

JUDGE GALLIGAN: I just had a real quick question before transitioning to that. This is Judge Galligan.

So how did the '054 patent fix the space issue somehow? I mean, did the inventors invent, like, a smaller buck converter?

MR. SHEASBY: So we did fix the space issue because we don't use an AMB, Your Honor.

We use single -- we use a single FPGA. And if you give me your notes, I'll read to you those passages.

What we do is we talk about a number of techniques for solving space. And give me one second. I'll read to you where those are.

JUDGE GALLIGAN: Thank you.

MR. SHEASBY: If you talk to column -- if you look at column 23, lines 1 through 15, we move the flash to an internal FPGA to make the space smaller.

And in fact, we quote that this saves physical space. We also don't use an AMB which is a very, very large chip.

We use instead a combination, primarily an FPGA which has a number of different functionalities built in a NAND which makes it smaller.

So the way we've solved the space problem is through this FPGA with internal flash. And the specification talks about that at 23, 1 through 15.

May I continue, Your Honor? Or did you have another question on the subject?

JUDGE GALLIGAN: Yes, thank you very much.

MR. SHEASBY: Okay. So I now want to talk about this VTT issue.

And this VTT issue to me is fascinating. And the reason why it's fascinating is because it's an argument that plaintiff is whipsawed on or Petitioner is whipsawed on.

So Petitioner is saying, well, when Harris says you're replacing VDD with a pin -- you're replacing VDD with an on-module power management, that would mean VTT as well.

So that's an argument they made. By the way, that's a new argument but I'll take it because if Harris is saying VDD is also VTT, they only describe a single voltage regulator module that can do VCC, VDD, and VTT.

That argument weighs in favor of Patent Owner. But the reality is, is that the reason why Harris doesn't speak about doing VDD is because Harris is very focused on local conversion for the buffer and for the DRAM.

But VTT is not in the buffer, and VTT is not in the DRAM. VTT terminates on the module.

Dr. Mangione-Smith -- and once again, this is unrebutted in any substance -- in substantive evidence at paragraphs 96 and 97 of Exhibit 2031 speaks about the fact that VTT is a daisy chain.

It needs to be on the board because VTT is controlling every DIMM in the board.

And so the idea that VTT may be different on one module than it is on another module would make it impossible for VTT to be synched across all of the modules.

And so once again, this idea that there would be a motivation to add VTT, this is just using our patent claims as a road map.

Someone sat down and said, let me pick out a random voltage and select it into one of my combinations.

Doing VTT on module would destroy the entire purpose of VTT which is to control all the modules together.

And in addition to that, it's based on what I think is a significant misreading of the JEDEC specification.

This is Exhibit 1026 at page 49. What this speaks about the fact is there was some argument that VTT -- it's actually indirect.

VTT in the specification is based on VREF. There's no argument that VREF would come in as a separate converter.

By the way, that's just arbitrary that they didn't choose that one. They could've just as easily choose that one.

But they didn't want to because they didn't want to show that their argument leads to some situation which there's eight separate converters on the module.

But I want to show you something in particular of note too. The value of VREF may be selected by the user to provide optimum noise margin in the system.

That is actually the warrant for what Dr. Mangione-Smith is talking about.

Dr. Mangione-Smith talks about the fact that VTT is always done at the board level because you want to control all the modules together.

And that VTT may be traditionally something approximating half of VDDQ.

It can be set by the user. So you put VTT on the module because you want to have the ability to control them altogether.

There was some argument and I want to get it precisely. Give me one moment. I'm going to go to slide 19, slide 20.

MR. CHANDLER: Judge Galligan, I just want to note. Sometimes I couldn't hear your questions.

If you could move your mic down a little when you're asking your questions. I had some trouble hearing you. Thank you.

JUDGE GALLIGAN: Thanks.

MR. SHEASBY: Harris talks about the fact that it wants to be technologically independent.

This was an argument that they made for why VTT should be on module.

There are two points to that. What Harris actually says is they want the memory devices to be technology independent.

VTT does not go to the memory device. There's this confusion in the specification -- in the petition.

They suggest that VTT goes to the memory device. Harris is concerned with technology independence on the memory device.

This Exhibit 1026 at 1 is the pin out for a DDR SDRAM. You will look all day. You will never see VTT on that.

VT does not go to a DRAM. Harris is about technological independence for the DRAM.

It says nothing about stripping the system of its ability to independently control -- to control jointly all the devices together.

And so what you've done is when you weigh the evidence, you can weigh it in two ways which is you have Dr. Mangione-Smith explaining exactly why VTT is never generated on module because it must be controlled across the entire system.

You have this mistaken understanding that VTT would ever go to the DRAM.

It never goes to the DRAM. And you have this misreading of Harris.

Harris doesn't say technological independence for the module. Harris says technological independence for the memory device itself.

Next issue, VDDSPD. Okay. Once again, we have Harris actually doing what we're debating.

How do you implement his invention onto an FBDIMM? We have no reference to VDDSPD as being some type of separate voltage that will be created or created by a separate module.

Dr. Mangione-Smith speaks at length about why VDDSPD which by the way once again doesn't go to the memory device.

And so that argument that Harris talks about technological independence, that argument does not apply because Harris talks about technological independence for the memory device, not for the SPD.

The SPD must be controlled and the voltage must come from the motherboard because once again the bus for VDDSPD is on the motherboard.

Just to sort of give you some context, SPD is about the motherboard being able to understand what type of device has been plugged into it.

And what Dr. Mangione-Smith talks about correctly, I'm on slide 67, paragraphs 102 and 103 of his declaration, is this idea that you'd want to have VDDSPD on an individual device is just -- it's nuts.

It's hindsight. The whole idea is for there to be one VDDSPD on the board so that you can monitor all the devices together based on that bus that's on the board.

And so once again, this is using hindsight bias to create the roadmap for the system.

Let me stop there. I've spent a long time, but that was crucially important.

Are there any questions that I've egregiously failed to answer for Your Honors?

JUDGE JURGOVAN: What is the VTT actually used for?

MR. SHEASBY: VTT is used to terminate the -- it's used to terminate the -- all the devices.

So VTT is when power goes too low, you shut off everything. And so it's the Board saying wait a minute. There's not enough power coming in. Stop.

And the Board makes that decision. The termination occurs on the module.

But the Board makes the decision as to when to stop. So the Board needs to know how much power is going -- there needs to be consistent power going to each of those.

VTT needs to be consistently going to each of the FBDIMM modules so that the Board can make the decision when to shut off because the Board needs to shut off everything at the same time.

It can't have individual devices turning on and off because the individual devices are being addressed together in many situations.

And that's in the record. Dr. Mangione-Smith talks about that at 96 and 97 what the purpose of VTT is, Your Honor.

JUDGE JURGOVAN: Thank you.

MR. SHEASBY: Okay. So I'm going to go over my time. But I think it's worth it.

The next issue I wanted to discuss and I'm going to jump around a little here hopefully with a little more alacrity than I have in the past.

I want to talk about the PCB interfaces. And this is a situation in which I think there seems to be ships passing in the night.

So this is not an obviousness issue. They're claiming that this structure of edge connections that couple power data address and control signals between the memory model and the host.

They're not saying that's obvious. They're saying that the FBDIMM specification teaches that, full stop.

That's the evidentiary issue, not whether to be obvious to do it or whether the specification teaches about it.

This is another situation, Your Honors, where it's not someone -- some sort of an inventor was sitting with -- on the beach and thinking, wouldn't this be great. Let me write this limitation and add it in.

This is one of the central issues, the insights of this patent, the '918 patent.

If you look at Figure 4B, if you look at column 12, lines 24 and on, this idea of having a memory controller that sends signals without intervention of any other chip between the system, the MCHs on the system and the actual memory module, there's a core inside of this patent.

It's not some random limitation. It's not some little thing. It's one of the key aspects, a single bus interface that couples the MCH, the DRAM with nothing intervening between it.

Okay. So now let me explain why I'm giving you this speech. This is what they say is that bus, the edge connections that add control signals.

This is -- I'm on slide 23. The top of their document is -- top of it is from their petition.

They say the control signals and the address signals are A0 through A15.

And the control signals are those listed below. Those signals only exist from the AMB to the memory.

The AMB is on the modules. Those signals do not exist from the memory controller to the AMB.

They say, oh, it's no big deal. This is the AMB. It's doing a translation between the memory module. It's the same difference.

It's not the same difference. The inside of this patent, there's no intervention between the memory module and the signals going to the devices.

They don't want something in between to translate. And if you look at what the admission of their witness is, is that the information is sent by serialized packets.

A serialized packet is not a signal. And any argument that a serialized packet is the same as a signal or a serialized packet is equivalent to a signal, none of that in petition and that's an improper new argument that should not be allowed.

And there's a reason why there's such a profound difference between the signal-based approach and the FBDIMM-based approach.

This is Netlist Exhibit 240, and this is at page 99 -- sorry, at page 109.

And what it talks about the fact is the FBDIMM uses a unique interface.

That unique interface is the situation of which it doesn't -- it sends packets as opposed to individual signals.

And that unique interface leads to very profound latency problems at lower utilization rates.

In other words, this insight of using signals as opposed to serialized packets is a break and departure from FBDIMM.

And this argument that we cover FBDIMM, that argument is not in the record, in their petition, and it is not what our patent says.

We cover the form factor, the shape of the board of an FBDIMM. There's nothing that indicates that we are covering FBDIMM.

You may think I'm picky. But at some level, trials matter and what you write in a petition matters.

I'm on slide 23. What they're pointing to as the control signals do not come from the board memory controller to the module.

They are created at the advanced memory buffer. It's not a distinction without a difference.

It's a critical insight of this patent that the signals come uncorrupted from the module on.

Your Honors, I'll stop there. Does anyone have any questions about that one?

JUDGE GALLIGAN: Just a quick -- this is Judge Galligan. Just a quick question. I hope everyone can hear me.

You said that the patents cover FBDIMM. Can you just be more specific. I don't see that in the claims.

MR. SHEASBY: The patents do not cover --

JUDGE GALLIGAN: The form factor?

MR. SHEASBY: Yes. So --

JUDGE GALLIGAN: Where is that in the claim?

MR. SHEASBY: It's not. So to be clear, I don't think these patents cover FBDIMM at all.

My brother says you have to interpret these patents to cover FBDIMM.

That's his argument for why an AMB counts as a sign going from the board -- from the off-board controller -- from the controller to the memory module.

I'm saying that is not what the patent teaches. The patent does not teach that you are encompassing an FBDIMM.

It's saying, you use the FBDIMM board shape, the form factor. But he's trying to escape this failure of evidence that you see on slide 23 by saying you have to interpret the patents to cover this.

And my point is no, you don't, for two reasons. One, the patent talks about FBDIMM form factors, not FBDIMM AMBs.

Two, it's a central insight of this invention beginning at column 25 for there not to be an intervention between the offboard module and -- the offboard memory controller and the module. Does that answer your question, Your Honor?

JUDGE GALLIGAN: Yes, thank you. And then one follow-up question.

When you said -- when you were talking about there's no intervention, which claim limitation is that directed to, please?

MR. SHEASBY: It's the first claim limitation, the interface including a plurality of edge connections configured a couple power data address and control signals between the memory module and the host system. The control signals must come from the host system.

(Simultaneous speaking.)

MR. SHEASBY: And the control signals they point to on slide 23, those are not on the host system.

Those do not come from the host system. It is a failure of evidence in their petition.

I'm going to have to skip around a little and do some broken heels running, Your Honors.

The next issue I wanted to discuss is Spiers. Oh, actually, the next issue I want to discuss is Amidi.

I'll spend just a few minutes on Amidi not because it's not important but because once again this concept of using the patent as a road map.

Harris speaks about redundant voltages. Harris doesn't care where the redundant voltages come from.

They can come from battery. They can come from anywhere you want.

You can have redundant voltages in Harris. The petition arbitrarily proposes that the redundant voltages in Harris would use Amidi with the battery on module.

But there's no explanation in evidence as to why the battery on module would be a desirable strategy as opposed to the battery being off module which is what Harris would contemplate.

It doesn't care where you get your external voltages from. It can be on module or off module.

And in fact, there are strong reasons to keep the voltage, the battery off module.

Once again, these are undisputed in the record, paragraph 108, paragraph 109 of Mangione-Smith.

In fact, the specification, our specification teaches about the noxiousness of having the battery on the module itself.

For example, at 4, 56 through 58 and it does so at a later point in time in the specification as well.

It is simply hindsight in which they're trying to create the claim limitations from the reference by putting the Amidi battery on module. Next --

JUDGE GALLIGAN: Counsel, if it's such a bad idea, why does the patent do it? Is there some --

(Simultaneous speaking.)

MR. SHEASBY: Oh, you mean why does Amidi do it?

JUDGE GALLIGAN: Oh, the patent does not do it? Okay.

MR. SHEASBY: Patent does not do it. The patent -- as my daughters would say, the patent throws shade at putting the battery on module.

It does that at column 4, lines 56 through 58. And let me find the other portion where it does that.

If you'll give me one second, Your Honor, I will find that for you.

It's also at column 26, 1 through 9 where the patent speaks about the fact that there's significant deficiencies from putting the battery on module.

The point I'm trying to make is that the petition just uses the Lego approach in which it finds things and puts them together without any rational explanation that stands up at trial as to why they would be put together.

Add the Amidi battery to the Harris module. Harris says you can have any external power source you want which would include a battery.

What's the explanation for why after Harris says use any external battery power you want to put the battery on the FBDIMM module that already has a converter on it and deal with the thermal and form factor constraints of having that battery there?

We know this. That was both battery supported DIMMs before it invented this technology right now.

They're terrible. The industry found that out after us. And we speak in our patent as to why this is such a bad idea. But it's arbitrarily combined together by the Petitioner.

JUDGE JURGOVAN: One minute left in your time. You can continue, but you'll be eating into your rebuttal time.

MR. SHEASBY: I appreciate that, Your Honor. I am going to continue, I think.

JUDGE JURGOVAN: Thank you.

MR. SHEASBY: I'm going to speak about Spiers now. This is, I think, grounds 4 and 5.

And once again, I want to come back to this language in the claims.

A plurality of edge connections configured to couple power data, address, and control signals between the memory module and the host.

There's this huge debate about how Your Honors should construe memory modules.

I'm not going to discuss it today. And the reason why I'm not going to discuss it today is because it's fully briefed and it's irrelevant.

And the reason why it's irrelevant is in two pieces. There was some argument that the Amidi was a memory module.

And therefore, it's irrelevant whether Spiers is a memory module.

That's a new argument that should be forbidden and rejected. In the petition, the memory module is Spiers, this PCI device.

And basically, what the petition said is that anything that had memory on it is a memory module.

That's what they say. That means a graphics card, a gaming console, a motherboard, my phone, these computers that were on right now, all of those are memory modules.

That's an absurd position. Whatever memory module means, it does not encompass the breadth of what the petition sets.

In other words, you don't have to set the outside boundaries of what is or is not a memory module to recognize their evidence just because something has memory on it, it's a memory module that makes evidentiary sense.

In this situation, it's very important to keep in mind two things. We talk about control signals going from the host to the memory module.

It's required. We know that's required from the claims. We also know that Petitioner wants this to be a JEDEC-compliant design.

They want to use DDR. If you talk about Mangione-Smith at paragraph 53, he talks about the way that DDR receives control signals.

There's a memory controller that receives unadulterated address and command signals to the DRAM through a data bus. This is going to become very important in a moment.

This, page 131, is what Harris actually is. Harris is its own system.

They call it a backup device. But on that backup device, it has a power supply where the conversion happens.

It has a processor, it has an interface, and it has volatile and non-volatile memory.

What I'm going to show Your Honors is that the evidence in the record, the overwhelming evidence in the record is that the memory controller that sends control information to the volatile and non-volatile is at processor 160 that is on the module.

But the claim requires that the control signals come from off the module.

Let me show you this in a little greater detail. I'm looking at slide Figure 5.

Processor 198 sends the control and data and address signals to the memory modules which are in blue. And the regulators are in green.

Claim requires two things, that the regulators be on the memory modules. The memory modules are in blue.

And the control signals come from somewhere off the board. In this case, the memory signals are coming from on the board.

How do I know this? I know this because their witness admitted it.

In their petition, they recite the storage controller 132 as the memory controller.

Everyone agrees that a memory module has to receive control, address, and data signals from a memory controller.

And they say it's 132. We asked Dr. Wolfe, does that 132 provide any of the control signals to the NAND flash and PCI card?

His answer was no. That is fatal. The claims require that the control signals come from off module.

We asked him again. That was slide 128. This is Wolfe at 214:23 to 215:2 in his deposition.

Slide 129, does the memory controller which in the storage controller 132, that's that one that's off board, does that provide time and control signals to the flash for the DRAM? The answer is no. He admitted it under oath.

132, the only memory control that provides timing and control signals is the processor within 198.

This is slide 132. He admitted that again and again and again. The control signals are coming from that processor.

That processor 198 is on the module. The claims require that it be off module.

It's a fatal defect. What's the move they make? The move they make is to say, oh, this is just like an FBDIMM situation.

First off, that argument is not in their petition. It should be rejected.

Second of all, our claims do not cover FBDIMMs. Third, as we discussed, this insight that we talked about that the control signal is coming unadulterated from the host system to the memory module with any intervening structure is not just some random language that someone put in.

It's not just a puff piece. If you go to column 25, the MCH -- in the build of the MCH on its own to capture that is a critical aspect of this invention.

I now want to talk about how this goes deeper into Spiers just briefly.

JUDGE GALLIGAN: Counsel, this is Judge Galligan. I had a quick question on that.

So looking at the '918 patent or either one of them -- but in the claim -- to that slide right there, in the claim when it says that it receives power, data, address, and control signals, is it the Patent Owner's contention that the memory modules in the prior art don't receive power, data, address, and control signals from the system?

MR. SHEASBY: From Spiers? Yes. That is absolutely our contention.

And it's not just our contention. That's what -- if I could go to slide 129.

That's not just my contention. It's what Dr. Wolfe admitted under oath in his deposition.

JUDGE GALLIGAN: I'm saying at all. So for instance, that previous slide you have, 104, the claim requires and one of the claims says that it coupled to receive power, data, address, and control signals.

And I don't think it later then says what the signals have to do. So is it Patent Owner's contention that there are no power, address, and control signals that go to the identified module in Spiers?

MR. SHEASBY: Yes, that's what Wolfe talked about in his deposition that the timing control signals for what Spiers does which is have memory and flash is on the control.

And I actually -- I can actually show that to Your Honor if you give me one moment.

So you can go to column 47 -- paragraph 47 of Spiers. What it speaks about the fact is that the processor on the backup device pulls read and write data from the bus.

But the control and timing signals are all generated internally by the onboard processor.

So I think if I could say this precisely as I can, the bus passes data signals.

But the control and timing signals, the control signals are all generated on the backup device.

And that's an intentional conscious part of the backup device. And so I think what Your Honor is suggesting is, well, can I read the claim so broadly as it just requires some control signal to come from the memory module -- come from the host system to the memory module.

Well, the control signals that they're pointing to in the petition are the control signals for the DRAM and NAND.

They're bound by the petition. It can't be some random control signal that's used for some other point.

The petition relies on the control signals for the NAND and DRAM.

The NAND and DRAM control signals are coming from the memory -- are not coming from memory controls and the storage control which is off module.

They're coming solely from the memory control that is on module.

So I would respectfully submit, Your Honor, that I can't make their case for them.

And they're bound by what's the in petition. That's why trials exist.

They point to control signals for NAND and DRAM. Those are not produced off module.

Those are produced by the processor on the card itself. Have I answered your question?

JUDGE JURGOVAN: But they are produced in response to a read or write command from the host controller, are they not?

MR. SHEASBY: So the host controller that the MCH pulls data -- so actually, I don't think that's right, Your Honor.

So the host controller is just feeding information to its storage. The backup device is going and stealing that write data and pulling it off as it's being produced and putting it into the RAM.

And so I don't think that's in evidence, Your Honor. I don't think that's -- first off, that's not what they say in their petition.

In the petition, their control are the control to the SDRAM and the NAND modules on the backup board.

But second off, I don't even think even if they would've made that argument that that would've flown under the evidence of what Spiers is actually doing. But that's not their --

JUDGE JURGOVAN: In some form, I mean, a memory controller has to be -- it has to have a control signal, read or write, to the memory.

It has to have an address of where it wants to write or read from.

And it must have the data that either is being read out or being written to.

But how can you say that there's no control signal coming in to the memory module from the memory controller or there's no address or there's no data?

MR. SHEASBY: Well, so that is separate from address. I don't think anyone considered data and address to be a control signal. They're distinct.

JUDGE JURGOVAN: No, no. The read or write would be the control.

MR. SHEASBY: Right. And what I'm telling you is that the control signal they point to is the read or write to the NAND and DRAM. That is generated on module.

JUDGE JURGOVAN: Yeah, but in response to what?

MR. SHEASBY: In response to nothing. The backup device is flowing -- is sort of spying or sort of wire sharking the data flow from the regular system and pulling it off in real time and then doing with it what its processor tells it to do.

JUDGE JURGOVAN: I see what you're saying. In other words, it's a read and write stream coming into it that is just monitoring.

And it will pull off -- if it's told to by the memory controller, it'll pull off a read or write and store the data. Is that what you're saying?

MR. SHEASBY: It pulls off literally everything in Spiers. The off module memory controller is not telling it to do anything.

It's just taking everything. And the processor on the PCI is what's telling it what to do.

JUDGE JURGOVAN: I see.

MR. SHEASBY: It being the memory. By the way, we sell these cards, Your Honor.

These are the things that -- this is not a memory module. These things that they're describing, these are little computers. That's what they are.

JUDGE JURGOVAN: Okay. Thank you.

MR. SHEASBY: Sure. I want to talk about one other issue, and that is that the same arguments and defects that I believe exist in using the voltages as a roadmap also exist in Spiers.

And let me tell you what I mean by that. This is their mapping for Spiers.

I'm on slide 147. Do you see how they're having VTT going to the DRAM bus?

That's not -- their combination is not Spiers plus Amidi plus DDR chips.

Their combination is Spiers plus Amidi plus a memory module. I know that because it requires VTT to DRAM bus.

VTT to DRAM bus is not something that is ever on a piece of DRAM.

VTT to DRAM bus is something that is solely, solely, solely on the memory module.

So even their memory module mappings, their mappings for these voltages which I think are just hindsight 20/20, they're not -- they get -- they're actually putting an entire JEDEC module, not just DRAM on there to get some of these voltages including VTT.

But it's the same arguments that I've made before for the DRAM about VTT and VCC, the different types of VCCs going to different locations.

All of this is hindsight bias. There's nothing that requires there to be multiple converters to do it at the same time.

There were significant detriments to using multiple converters. And in fact, their combinations make clear that Spiers is not the memory module.

But the memory module is the module with the VTT to DRAM bus that's on it.

Your Honors, I do have to reserve some time. I'm very sorry I couldn't talk to you more about this. But I do have to reserve some time for my surreply.

JUDGE JURGOVAN: Thank you. You have 15 minutes left for your surrebuttal.

And we'll hear from Petitioner now your rebuttal. You have 30 minutes.

MR. CHANDLER: Thank you, Your Honor. May I -- Mr. Sheasby, could I please share on the screen?

MR. SHEASBY: Oh, yes, yes.

MR. CHANDLER: All right. Judge Jurgovan, can you see my screen, slide 102?

JUDGE JURGOVAN: Yes, I can. Thank you.

MR. CHANDLER: Thank you. So I'll pick up with Spiers. The last point by opposing counsel was not an accurate description of how Spiers works.

Judge Jurgovan, you had it correct. The way Spiers works is there's a storage controller 132.

As explained by our expert in the upper right, that is the memory controller.

That is what sends the read or write commands to the memory module in the bottom right.

You can see that in paragraph 34 in the bottom right that the storage controller 132 stores a copy of the data in the backup device 144.

And you can also see it on our slide 115 on the left-hand side is the PCI standard which permits both read and write.

But then on the right-hand side of the slide is Figure 9 of Spiers which talks specifically about the host computer being able to both store memory in the DRAM but also transfer memory out of the DRAM which would be a read command.

So it's 132 on Spiers which is the storage controller on the host that satisfies the memory controller.

I want to respond to the argument about some of the testimony about Spiers and 132.

So Netlist is trying to argue that Figure 5 of Spiers on the right is not a memory module because according to Netlist, the only memory controller according to them is 198 which is the processor.

And again, that's incorrect. The storage controller 132 is a memory controller on the host computer as I just showed you on our slide 102.

And then with respect to the expert testimony that they referenced on their slide 129, the testimony from our expert was very precise about how this works.

Our expert explained the storage controller 132 does not communicate directly with the memory devices.

Instead as Judge Jurgovan correctly recognized what happens is storage controller 132 sends data, address, control signals that are received by processor 198 which is on the memory module.

And then processor 198 sends the corresponding data, address, and control signals to the memory devices.

132 is still the memory controller that calls the shots, but it communicates those signals to the memory devices through processor 198.

This is a very common arrangement. It's how FBDIMM works, and it's how other memory modules work as well.

If we look at their slide 128, our expert was making the same point on this slide.

Again, storage controller 132 doesn't communicate directly with the memory devices.

It communicates indirectly through processor 198. That doesn't change the fact that Figure 5 of Spiers is still a memory module.

I think it's important to keep in mind that Netlist's claim construction arguments rely almost entirely on extrinsic evidence and fail to identify intrinsic evidence supporting their proposed construction.

The arguments that I saw that the slides were flipping through very quickly, there was one slide 108 that has the claim language and the next slide, 109, that has a little bit of a quote from the intrinsic evidence.

But it cuts off what that intrinsic evidence actually says. And so I thought it could be helpful to actually look at the rest of the sentence that they cut off.

And so if you look at -- I'm having a little trouble there. I'll go to the other patent here.

If you look at the '054 patent and it's the same cite in the '918 patent.

At column -- at the bottom of column 3 is the sentence that they started to quote.

So at the bottom of column 3 starting at line 65, described herein is a memory module couplable to a memory controller of a host system.

Then it goes on to say the memory module and we go to the top of column 4 includes -- and then it goes on.

And it talks about a couple of things. One of the things that the memory module can include is a controller.

And what does that controller do? The controller on the memory module receives commands for the memory controller on the host.

And then in response to those commands from the memory controller on the host, the controller on the memory module can operate the non-volatile memory and the volatile memory and transfer data.

And it's all done based on at least one received command from the memory controller.

This is important because it's intrinsic evidence that Spiers and the fact that Spiers has processor 198 on the memory module that receives the commands before forwarding them on to the memory devices.

The set up of Spiers matches the set up in the patent for what a, quote, memory module is.

A memory module can have a controller on the module that doesn't take away from the fact that it's still a memory module.

If we go back to our slides 101 in the upper right, this is the District Court's claim construction.

The District Court, all it said is that a memory module includes the structure necessary to connect to a memory controller.

Spiers certainly has that. There's a bus 128 to connect to the storage controller 132.

And it's the storage controller 132 that is going to send or receive the memory commands. Before I go on to the next subject, any questions on that issue?

JUDGE JURGOVAN: None from me. Thank you.

MR. CHANDLER: All right. There was some discussion about VTT not being supplied to the memory device or something along those lines.

That's a new argument that Patent Owner is making that VTT doesn't go to the DRAM.

That's incorrect as shown on our slide 54 in the upper right. So VTT, we've put in a red box.

And as you can see, VTT if you follow the wires is coupled to each of the SDRAM memory devices on the memory module.

And VTT needs to be couple to each of the SDRAM memory devices to terminate the address, command, and control signals.

With respect to does Harris teach generating VTT on the memory module.

The answer is yes because Harris teaches generating all the voltages that you would need for a memory module.

And we know for an FBDIMM with DDR memory devices that VTT is one of the voltages that you need to use.

And so if logic follows, it would be obvious if you're following the teaches of Harris to generate all of the standard FBDIMM voltages on the memory module.

Harris says there are 28 VDD pins. If you look at the FBDIMM standard, the way that those 28 pins are divided is 24 pins for VDD with four pins for VTT.

So the way you get to 28 pins is there are 4 pins for VTT. And what Harris is saying is let's get rid of all of those 28 pins plus all of the other power pins, replace them with only six 12-volt pins for power and then generate on the module using buck converters all the different voltages that are required.

This was commonly done. There were chips as shown on slide 55 that were specifically designed for that purpose.

And furthermore, as shown on slide 57, the reason that Harris teaches generating all the voltages is because that provides for technology independence.

When a new generation of memory device comes out, you don't want to have to change all the voltages on the computer.

I'll go to this question about why would you use two different converters for the same voltage level, specifically 1.8 volts for VDD and VDDL.

And as a preliminary matter, that issue only applies to voltage mappings A and B.

That issue does not apply to voltage mapping C which has four different voltage levels.

And it's clear that when you have four different voltage levels, you need four different buck converters to output those four different voltages.

So to the question -- there was a lot of discussion, why would you have four buck converters.

The reason is that the FBDIMM standard which Harris specifically cites to, that standard teaches four different voltages that are needed by the module, that are needed by the memory devices on the module.

And therefore, Harris says generate all of those four different voltages on the memory module using buck converters.

That would require four different buck converters to output those four different voltages.

Now getting back to voltage mappings A and B, our contention is that even though VDD and VDDL are both 1.8 volts that it would be obvious to use two different buck converters.

This is discussed primarily on our slide 51. And the reason is to provide independent control.

There was some discussion by opposing counsel that the FBDIMM standard, their expert believes that the FBDIMM standard goes with this first option of using a single power converter.

However, the standard on the screen which is the standard for the memory devices that are used on FBDIMM provides two different options.

And thus, when you are implementing Harris and you're putting all of the voltage converters on the module when doing that, you would know from the JEDEC standard that there's these two different options and that there is a benefit to the second option which is independent control including sequencing of the power.

Opposing counsel made some reference to 10 milliseconds for startup time.

Let me see if I can pull that up. I believe it's their slide 42. Their slide 42, talking about 10 milliseconds, that's for an SODIMM.

It's not for an FBDIMM. Apparently, the SODIMM uses the option 1 approach where you use a single power converter.

But that doesn't take away from the fact that it was taught in the prior art and a person of ordinary skill in the art would know that there's a second approach which has its own benefits including sequencing the power, being able to turn power on and off independently.

And it can be more cost effective to have multiple small regulators rather than one large regulator.

There was also some discussion about space. This is their slide 47.

So on their slide 47, they argue that supposedly there wouldn't have been enough space on the memory module for four buck converters.

There's nothing in the claims about space. The only thing that opposing counsel pointed to with respect to space is that they could put some non-volatile memory in the FPGA.

But there's nothing in the claims about that. What there is, is that as we described on our slide 48 -- as shown on our slide 48, our expert explained in the bottom right buck converters can be extremely small.

And paragraph 13 of Harris says that his invention can supply all of the voltage conversion within approximately one square inch, both sides of the printed circuit board.

And so to give a practical example, if you look at one of the buck converters that we cited, this is an example -- this Exhibit 1048, page 2, this is an example of both sides pointing to.

This is one chip with two buck converters, VOUT1 and VOUT2.

And if you look at the dimensions of that chip, it's 33.5 millimeters wide by 6.8 millimeters in the other direction.

And so that's 0.3 square inches. So 0.3 square inches is enough space for two buck converters with two inductors and two capacitors and the control unit for that.

So 0.3 square inches for two buck converters. That means that in the 2 square inches that Harris says is available on both sides to the FBDIMM, you could get up to 12 different buck converters in the amount of space provided.

So space is not a problem. It's never described in the patent as a problem.

It's never claimed as a problem. And again, our expert pointed out that these converters can be very, very small.

What else? There was a discussion about signals and the FBDIMM form factor.

So this gets to this question of whether data, address, and control signals from the host is satisfied by FBDIMM.

Opposing counsel admits that the patent describes the FBDIMM form factor as compatible with the invention.

That's significant because the FBDIMM form factor has fewer address and control pins because it uses these serialized, packetized signals.

That is the form factor of an FBDIMM. You don't have a dedicated pin for every address line and every control line.

Instead for the FBDIMM, a form factor, is you've got fewer numbers of pins for address and control lines.

And so the way FBDIMM works is it sends the address and control signals in packetized serial signals which the AMB on the module will then decode.

Those are still signals being sent to the AMB. If you look at our slide 35, the JEDEC standard follows those signals.

And if you look on slide 34, Netlist's expert admits that they are signals.

And again, the fact that the patent as shown on slide 37 admits that FBDIMM is a form factor compatible with the invention is significant because the FBDIMM form factor does not have dedicated pins for every address and control line.

Instead, it uses these serialized, packetized signals. There's also a suggestion that somehow our petition didn't make that point.

That's incorrect. If you look at, for example, the '918 petition, page 22, we explain that Harris in combination with the FBDIMM standards receives at 114 as I've highlighted in green the following signals.

And those signals include data, address, and control. We do not rely solely on the FBDIMM standards.

We also rely on the disclosure of Harris itself. We quote here, for example, paragraph 9 of Harris which talks about buffer/logic component 112 is provided for buffering command/address space as well as data space.

And those address and data come across 114 labeled memory control.

And then if we go on to page 23 of the petition, we specifically discuss the AMB JEDEC standard which, again, is talking about these packetized serial signals.

And we explain in both from the AMB standard that those are signals that run from the host controller or the DIMM.

I've only got a few minutes left. There are a couple more things I could talk about.

Are there any questions that the Board would like me to focus on in my remaining handful of minutes?

JUDGE JURGOVAN: None from me.

MR. CHANDLER: There's one statement that, opposing counsel, I do want to correct because, I mean, it's clearly wrong.

There was a question from Judge Galligan about space and the battery and how does the patent itself do it.

And I believe the response from opposing counsel was that the patent doesn't use batteries.

That's not really fair. The patent uses capacitors. And so, for example, I mean, if you just search for capacitors, you can see it throughout the patent.

But column 26 is referring to how the patent uses capacitors as the backup power supply in the event of a power outage so you can have enough time to transfer data from the memory devices over to the flash memory.

Capacitors are like batteries. In fact, they're bulkier and bigger than batteries which reinforces our point that space for buck converters was not a problem.

It's not discussed anywhere in the patent as a problem. And the suggestion that the patent doesn't use batteries is misleading.

It uses capacitors. Those capacitors take up some space. But as taught by the prior art, there's plenty of room for both buck converters and battery backup.

And in fact, if you look at our slide 31, Netlist's expert admitted that it was known in the art like Amidi teaches to have battery backup on the module.

You could have a side connection that goes to the battery backup.

You could still use the bottom edge connections to get from the host computer during normal operation.

This was a known configuration. And there was enough space to fit everything.

And again, if space was a concern, one of the strategies as explained on our slide 49 is that you can stack the DRAM memory chips because that will effectively free up -- you can use half the amount of space for the same amount of memory storage.

There's a question about sort of why do you have VTT. And VTT is for terminating the signals.

And that's important to permit the high-speed operation of these memory devices.

So as you get to DDR2 and DDR3, they're operating at faster speeds.

And the VTT is one of the signals that permits the faster speeds by providing the termination.

There's also -- there's some discussion about VDDSPD. And I want to correct a misstatement by opposing counsel.

Opposing counsel suggested that VDDSPD isn't used on the memory module.

And that's incorrect. As shown on the right side of slide 62 and as explained in our petition, VDDSPD is coupled to both the SPD on the memory module which is needed during startup.

But it's also coupled to the AMB buffer which you need to operate the module.

So VDDSPD is needed by the memory module. And therefore, under the teachings of Harris, there would be a motivation to generate all of the voltages that you need on the memory module.

And we know from the standard including the FBDIMM standard that one of the voltages that you need on the memory module is VDDSPD.

And that's why there would be motivation to include that as one of the voltages that you would put on the module.

If you didn't put VDDSPD on the module, that would be contrary to the teachings of Harris.

And then furthermore for ground 2 where we combine Harris with Amidi to get the benefit of battery backup, battery backup wouldn't work if some of your voltages are being generated at the host computer because the whole point of battery backup is when the host computer no longer is supplying power.

You want to be able to use the battery to generate everything on the module.

And VDDSPD is one of the voltages that you need on the module.

If there are no further questions, I think I'll try to get everyone to lunch a few minutes earlier.

JUDGE JURGOVAN: Thank you, Counsel. Let's hear a rebuttal from Patent Owner, 15 minutes.

MR. SHEASBY: Thank you, Your Honor. Give me one second. I'm having a little trouble getting my PDF. There we go.

I want to start with what was the actual evidence that led Your Honors to initiate this proceeding.

And the evidence that led Your Honor to initiating this proceeding was two things.

It was a portion of the JEDEC specification at Exhibit 1026. That was one of the two pieces of evidence that they cited, and they should be bound by that.

There is no second option of multiple converters generating the voltages.

The suggestion to the other was a gross misreading of the specification for JEDEC.

It's totally inconsistent with what Dr. Wolfe and Dr. Mangione-Smith.

How obvious was this? Let's do a thought exercise in which we accept that what I think is a gross misreading of the JEDEC specification.

Let's do a thought exercise. How obvious was it to put multiple regulators, multiple converters on the module?

It's never happened in history for an FBDIMM according to Dr. Wolfe and Dr. Mangione-Smith.

That's how obvious it was. This is objective evidence. But of course, it's a misreading of the petition of the document.

And the idea that there's a possibility of separate converters for VCC and VDD and the FBDIMM specification is an impossibility.

The specification only has one set of pins for VCC and one set of pins generically for VDD.

And those cover all those different voltages that they say it would be obvious to put on.

The argument that the observation that VTT never goes to the DRAM is new is, of course, incorrect.

On page 27 of our POR, this is for the '918. It makes clear that VTT goes to the terminators -- goes to terminators, not to the DRAM.

My counsel said that Harris teaches supplying all that you need. If Harris teaches supplying all that you need, we prevail because Harris teaches using one voltage regulator to supply all that you need.

Petitioner had time left on the record. He had time left to speak with you, and he did not debate or dispute at all the fact that when Harris teaches having additional regulators on module, what it's teaching is for the backups to have the backups, not separate and independent voltage lines.

He's teaching in Harris that it would just be redundant but still supply the same VCD, VCCD and VDD.

Silence speaks louder than words sometimes. Counsel had every opportunity to dispute that and they didn't.

The question about what a person thinks is obvious when they modify FBDIMM to add on module power is answered by Harris.

It's answered definitively. And by the way, if VDD includes VTT which is a new argument, that just proves our point.

Harris does not say you need a separate regulator for VTT and VDD.

Harris simply shifts it all across. The argument that our Micron evidence is SODIMM and is not FBDIMM is an entirely new argument that was made for the first time.

There was no dispute that the Harris teaching -- that the Micron teaching of tying everything close together as Dr. Mangione-Smith states applies to all the DDR2 FBDIMM modules.

Dr. Mangione-Smith talks about this at length at paragraphs 98 through 101 of his specification.

I want to talk about the space issue briefly. And the reason why I want to talk about it is it's not an argument that I can really have because other than a random passing statement in a deposition as opposed to in the petition which is where it needs to be.

And other than some fast mental math by my brother, there's nothing in the record contradicting Dr. Mangione-Smith's observation.

That's not just the gross square footage. It's the incredible complexity of having four different regulators on module that would deter a POSITA from doing this.

The thermal budget, not just the -- the thermal budget, the thickness of the chips which Harris expressly acknowledges is an issue.

We don't have to have a thickness limitation in our claim. The question is what would a POSITA be motivated to do.

And POSITAs were motivated based on the undisputed testimony of Dr. Mangione-Smith not to put massive number of regulators on their module as evidenced by what Harris did.

JUDGE BOUCHER: Mr. Sheasby, can I just ask? It's just been kind of nagging at me.

But why isn't this space constraints argument an unpersuasive bodily incorporation argument?

MR. SHEASBY: Yeah, so that's a good point that the Board is very hard on bodily incorporation.

And the answer is twofold. The first point is that the combination is the FBDIMM -- Your Honor, this is such an important question. Can I clarify? Do you mind? May I ask you a question in clarification?

JUDGE BOUCHER: Sure, that's fine.

MR. SHEASBY: When you say bodily incorporation, do you mean bodily incorporation of Harris or the space constraint argument? I may have misheard you.

JUDGE BOUCHER: I meant the space constraint argument.

MR. SHEASBY: Yes, okay. So that I can answer relatively easily which is that the motivation to combine that Petitioner points to is compliance with the JEDEC specification.

I'm on slide 34, paragraph 161. This is Dr. Wolfe. Dr. Wolfe is speaking about the fact that the combination is Harris plus the JEDEC specification.

It's not bodily incorporation because the combination requires you to go with the FBDIMM standard.

That's actually what Harris teaches. Harris is not looking to dramatically depart from the FBDIMM standard.

She's just adding an external voltage to it. So the reason why it's not just an improper bodily incorporation argument is because the combination requires you to fit within the imagination of what an FBDIMM would be under the specification with the strict thickness requirements, with the strict thermal requirements.

In other words, there's no analysis that the DDR2 and the FBDIMM could tolerate the amount of power that is used to provide four separate buck converters on a device with four separate inductors which is Dr. Mangione-Smith speaks about are incredibly expensive and complex.

So it's not unproper bodily incorporation because they are forcing this in to the FBDIMM box.

They could've come up with another combination. They did not.

They chose to use as their combination the FBDIMM specification, the exact thing that Harris already implements.

And Harris is not implemented in a way that they say anticipates the claims.

That tells you one thing. Harris was an extraordinary person of skill in the art at HP, gave it their best shot, and did not think it was obvious, beneficial, or desirable for there to be four separate buck converters providing four separate physical voltages.

He did not think it was desirable to have a separate VTT line. He did not think it was desirable to have a separate VDDSPD line.

All of these things that they spin, Harris did not do. That's the objective evidence before us.

I know you're not going to say I agree with you, but I want to make sure I've at least attempted to fairly answer your question.

JUDGE BOUCHER: Yes, that answers my question. I appreciate it. Thank you.

MR. SHEASBY: The next issue I wanted to talk about is what was dropped.

The patent specification is very clear about the importance of there being no interfering and this starts at column 25 between the MCH and the DRAM modules online.

That has profound implications for both why an FBDIMM interface which they rely on does not satisfy that requirement.

And slide 23, this is not a made-up argument that has no support in the specification.

It is the central part of our invention at column 25 for there to be unencumbered signals coming across.

They pointed to something between the AMB and the DRAM. Those are the signals they point to.

They are bound by that. They are bound by the consequences of that, Your Honor, and they can't run away from it.

This new argument that '054 column 5 allows for a processor within a processor, that is a new argument that was nowhere in their specification -- nowhere in any argument.

And it should be not allowed at this point in time, certainly not on a rebuttal case. The --

JUDGE GALLIGAN: This is Judge Galligan. I wanted to follow up on that.

In the '918 patent, the claim recites -- let me get the claim. It says there's at least one circuit coupled between the edge connections and the SDRAM devices.

And the circuit receives -- I'm summarizing here. It receives address and control signals via the edge connections and outputs control signals to the SDRAM devices.

So that seems to suggest that the patents allow -- I mean, the claim recites that there's something in between, right, at least in the '918?

MR. SHEASBY: '918? I'm sorry. What claim were you looking at again, Your Honor? I was rushing --

JUDGE GALLIGAN: Claim 1. And that's where I think Petitioner identifies in Spiers -- identifies the processor 198 as at least one circuit. That's the intermediary there.

MR. SHEASBY: Right. So it says a plurality of address and control signals.

And it says the address and control signals are coming from across the board.

And so if you're asking me can there be -- the way I read the claim as saying the address and control signals have to -- it does say address and control signals were divvied out to the original -- to the individual SDRAM devices.

And it does say a circuit does do that. But there still needs to be address and control signals coming from across the host interface.

And the problem with the FBDIMM interface, it's the same problem with the PCI interface as implemented in Spiers is that here there's an AMB which is creating the control signals and the address signals.

And in Spiers, what they point to is just the PCI. If you look at their petition, all they do is point to the PCI interface that talks about data and read.

That's all they point to is the evidence of there being control signals from the petition -- control signals from the host to the memory module.

But if you look at Spiers itself, you can't run away from this testimony.

In other words, if you look at their petition, they sloppily put up a generic PCI interface and say, look it, there's data on both sides. There's read on both sides. There's control on both sides. We win.

But the signals that are actually doing the control and timing into the DRAM which is what they're pointing to as the control signals are coming from the on module processor and that's with Dr. Wolfe.

So no one is suggesting that there can't be a chip on the module that's divvying these things out.

Those things exist. They're called buffers. And in more complex environments, there's other embodiments.

There certainly is a chip that's divvying it out to all the different DRAMs.

But the MCH at column 25, it is without any encumbrance sending control signals across the edge.

That's what the claim requires. That's what the embodiment requires.

So the problem is not that there's a second chip that's divvying thing out on module.

The problem is that first chip that is generating the address and control signals for the memory and Spiers is not off the module. It's on the module.

I should also point out that counsel has substantial time left on the record and did not engage at all my arguments about the fact that the VTT to DRAM bus that they're relying on is on the module and that they're in effect putting a module on this.

Nor did Petitioner who had excess time and could've argued, engage any of these issues that is just absolutely hindsight that you would need all these different converters to supply the different voltage.

There's nothing in Amidi and there's nothing in Spiers itself that teaches using all these different converters.

In fact, this is sort of ironic, Your Honors. But if you look at Amidi and I think this is going to be my last moment and then I'm going to run out of time.

If you look at Amidi, Amidi describes sending on single voltage to the DRAM.

That's it. The combination -- and let me find you that so I can put it in the record.

If you look at Figure 6 of Amidi, Figure 6 of Amidi after all this complex power does one thing.

It supplies a single voltage to the DRAM, to the module -- to the memory module itself.

And so this idea that Harris plus Amidi gets you three or four separate regulators, all of which are pumping separate voltages is just using the prior art as a roadmap.

That's all it's -- it's using our claims as a roadmap. There's nothing in Amidi and there's nothing in Spiers that teaches that many converters.

Amidi sends only one set of voltages, one pipe to the memory module.

And Spiers which does have extra converters because of the non-volatile and volatile does not send four to each of these different things. This is just a roadmap that's done. The last point --

JUDGE JURGOVAN: I think your time is up. If you can just finish up your point very quickly.

MR. SHEASBY: Sure.

JUDGE JURGOVAN: We'll conclude the hearing.

MR. SHEASBY: There are situations in which you have to balance expert testimony.

You have to weigh the facts, and it's a hindsight situation. Harris answers this question definitively.

It is the combination and that combination doesn't equal this patent.

Thank you, Your Honors, for your time. I so appreciate your engagement and your questioning.

JUDGE JURGOVAN: I want to thank counsel for a very interesting hearing, and we will now be adjourned. We'll go off the record.

(Whereupon, the above-entitled matter went off the record at 4:05 p.m.)

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